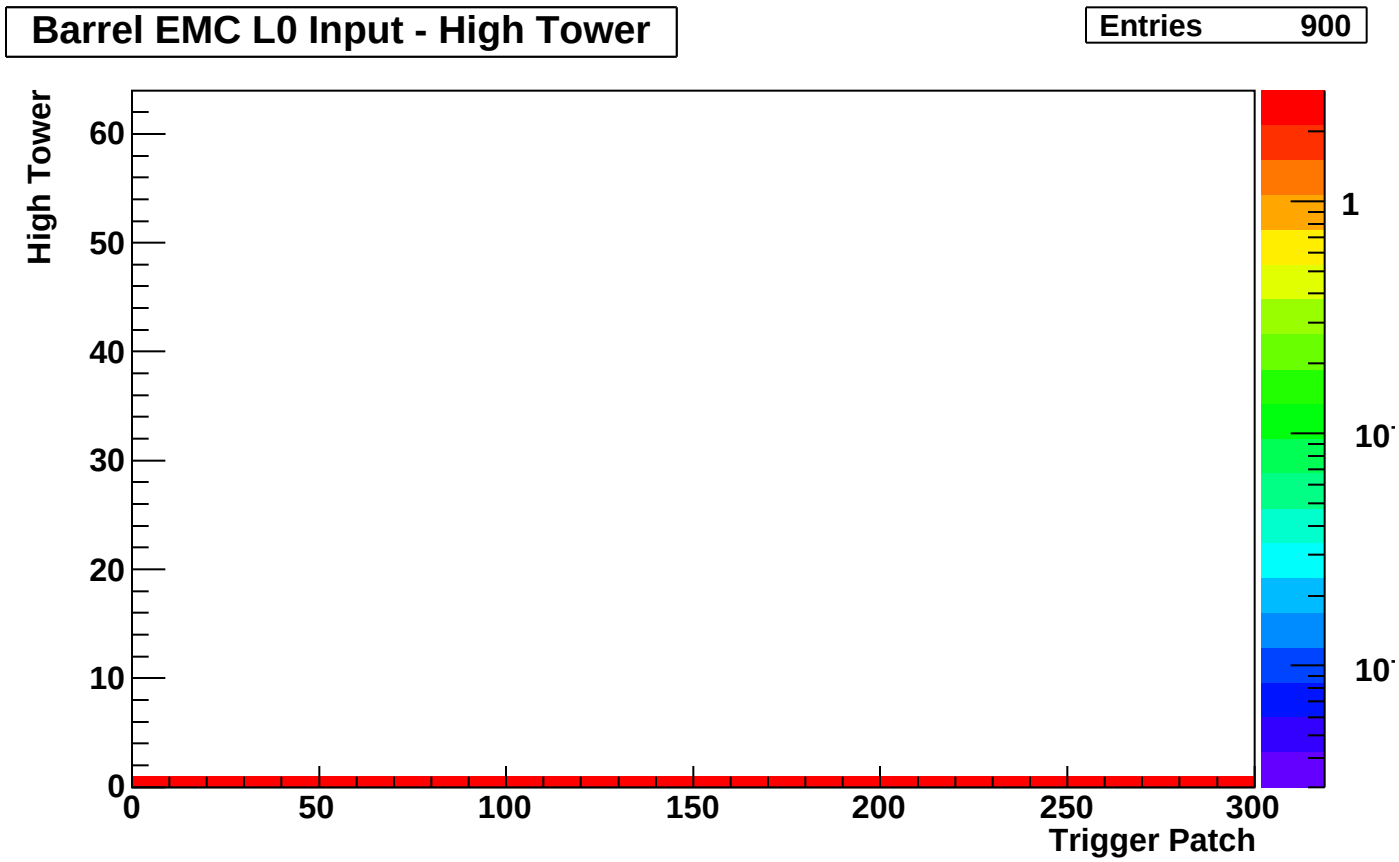
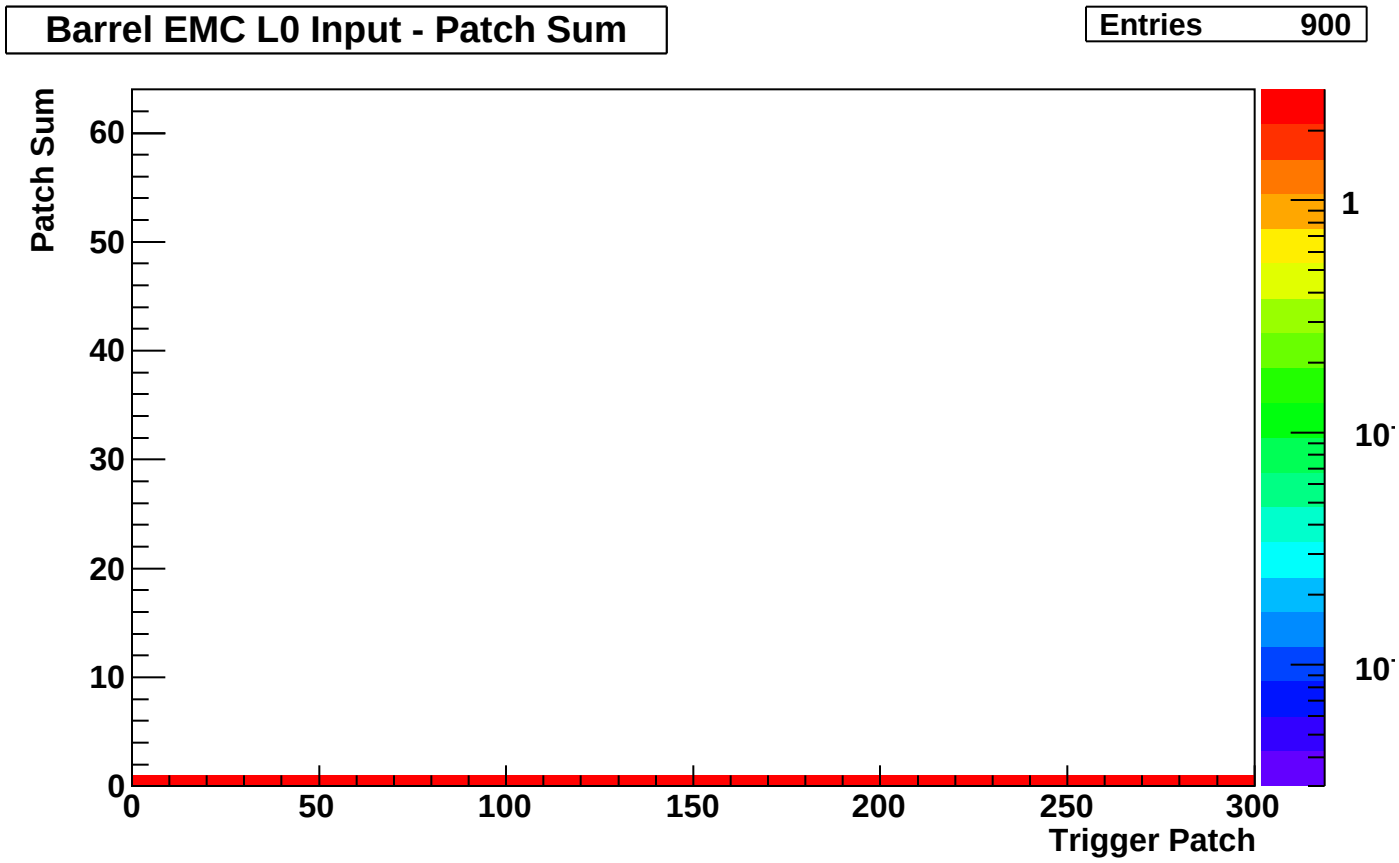
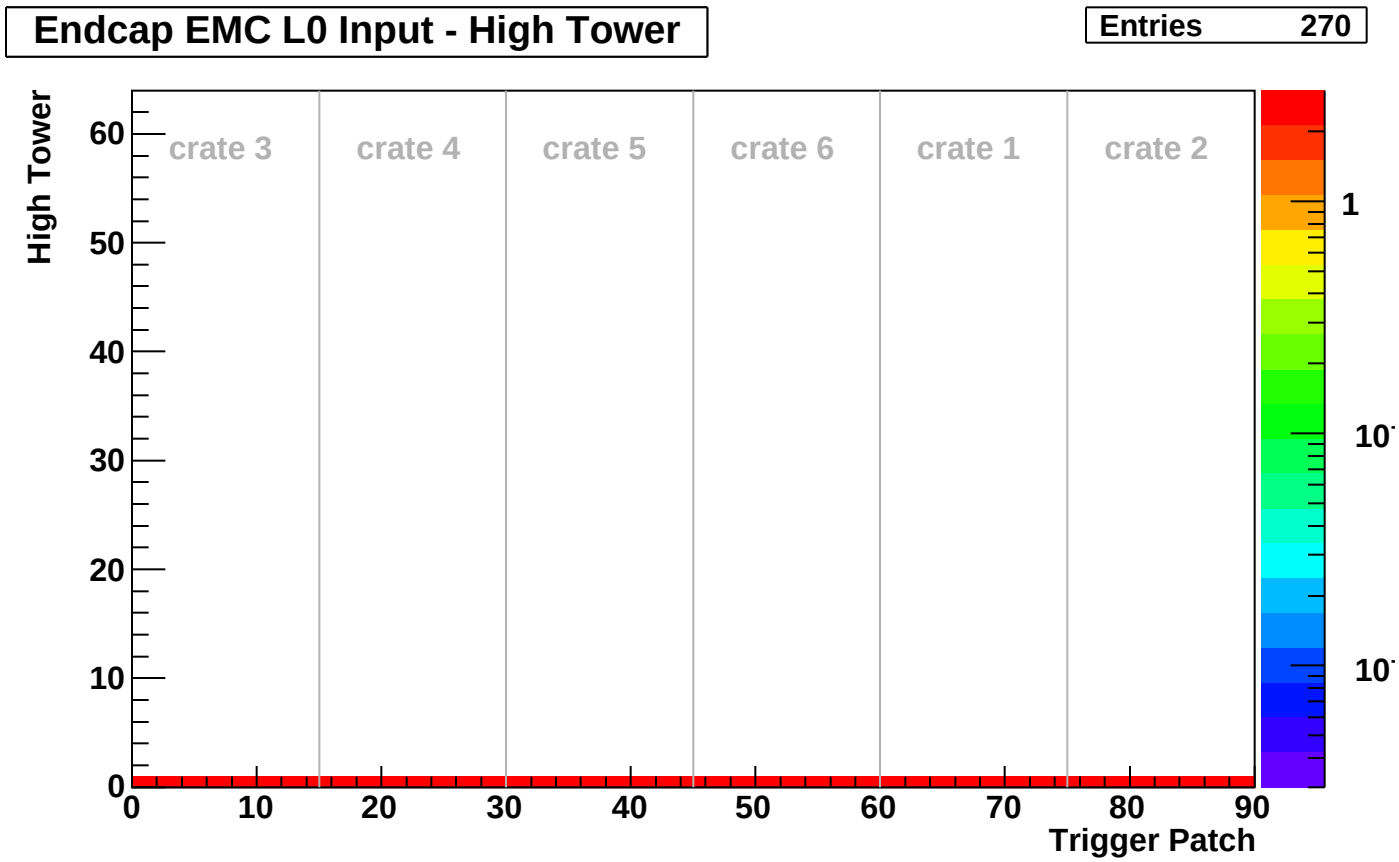
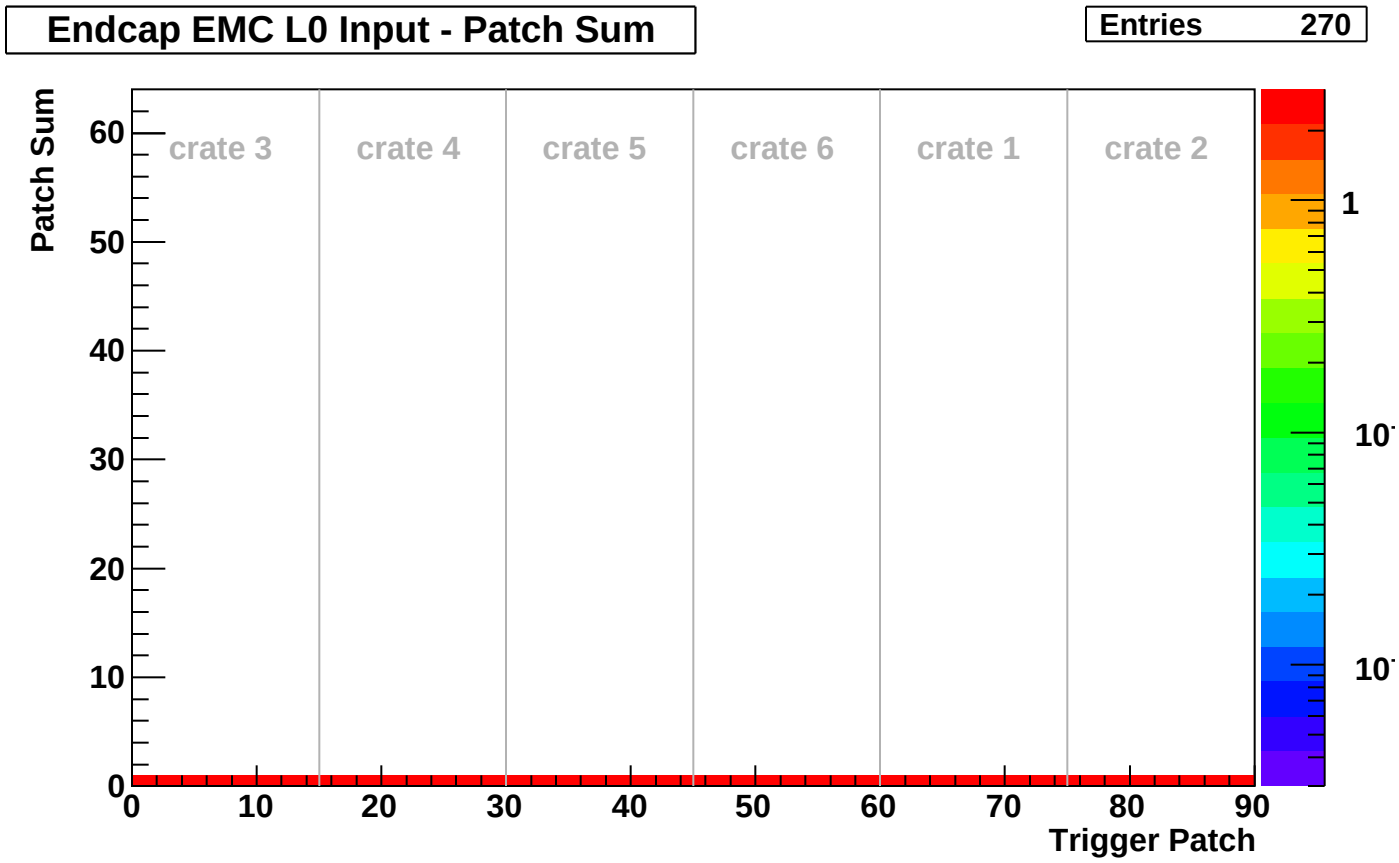
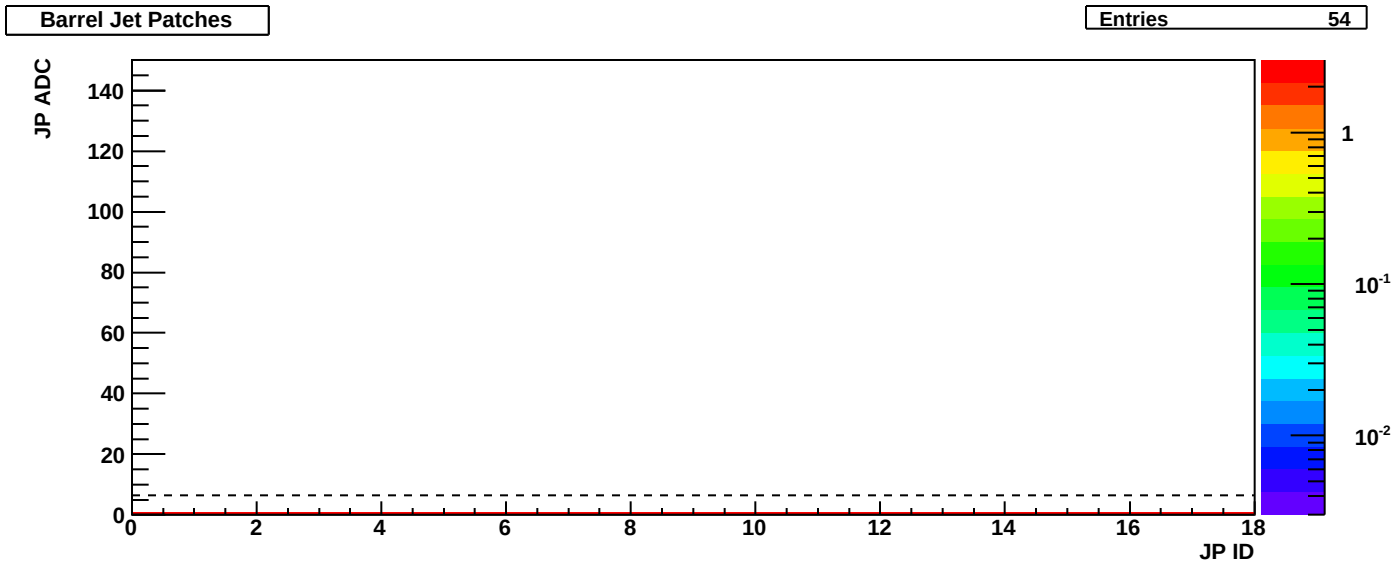
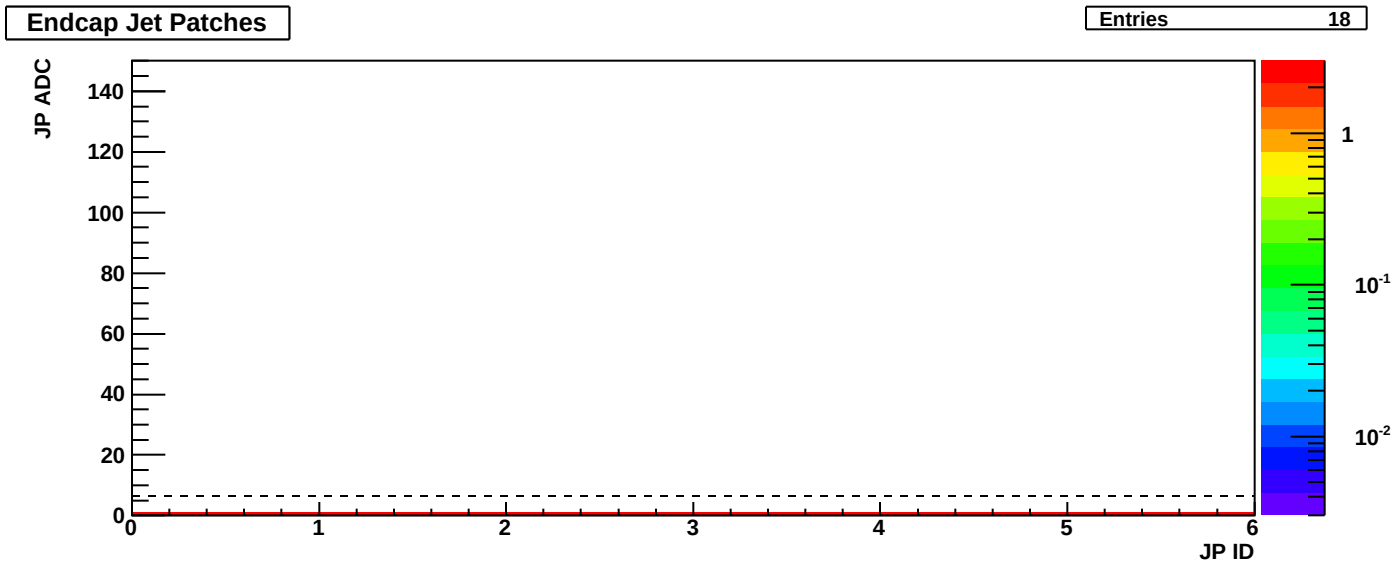

Barrel EMC L0 Input - High Tower
Entries 900
High Tower
0
10
20
30
40
50
60
0
50
100
150
200
250
300
Trigger Patch
1

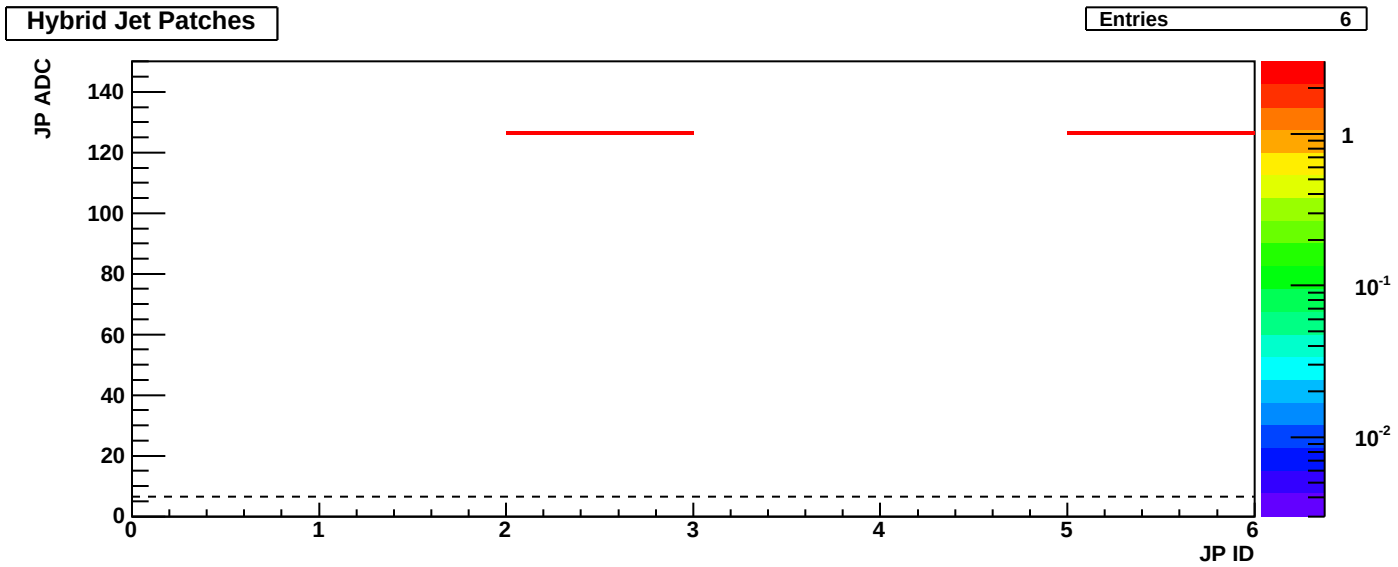

Barrel EMC L0 Input - Patch Sum
Entries 900
Patch Sum
0
10
20
30
40
50
60
0
50
100
150
200
250
300
Trigger Patch
1

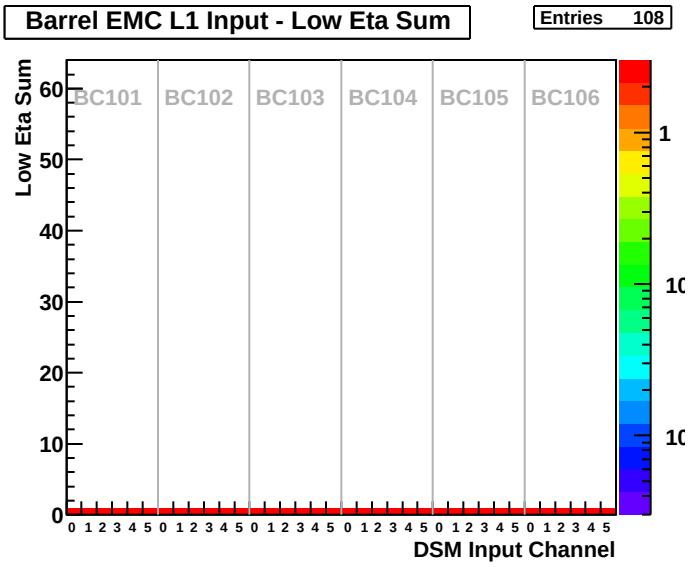

Endcap EMC L0 Input - High Tower
Entries 270
High Tower
crate 3
crate 4
crate 5
crate 6
crate 1
crate 2
Trigger Patch
0
10
20
30
40
50
60
70
80
90
1

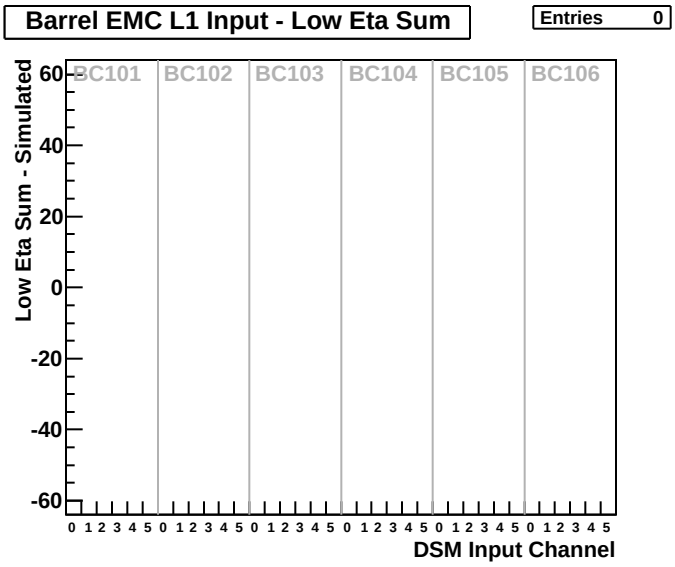

Endcap EMC L0 Input - Patch Sum
Entries 270
Patch Sum
crate 3
crate 4
crate 5
crate 6
crate 1
crate 2
Trigger Patch
0
10
20
30
40
50
60
70
80
90
1

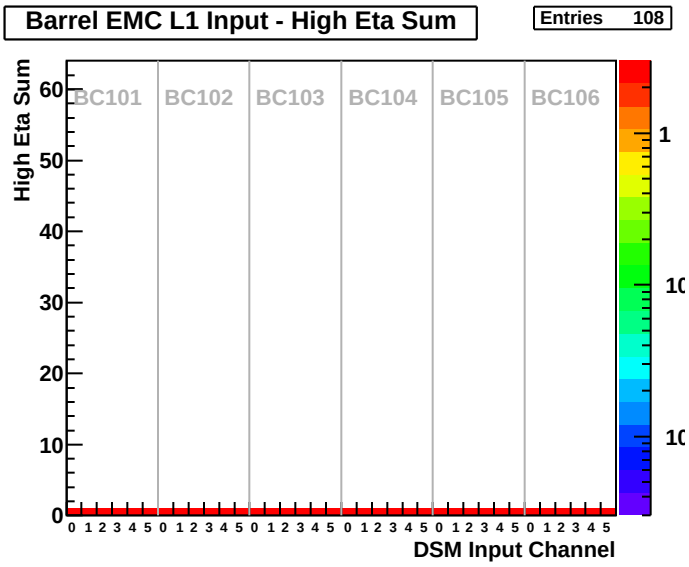

Barrel Jet Patches
Entries 54
JP ADC
JP ID

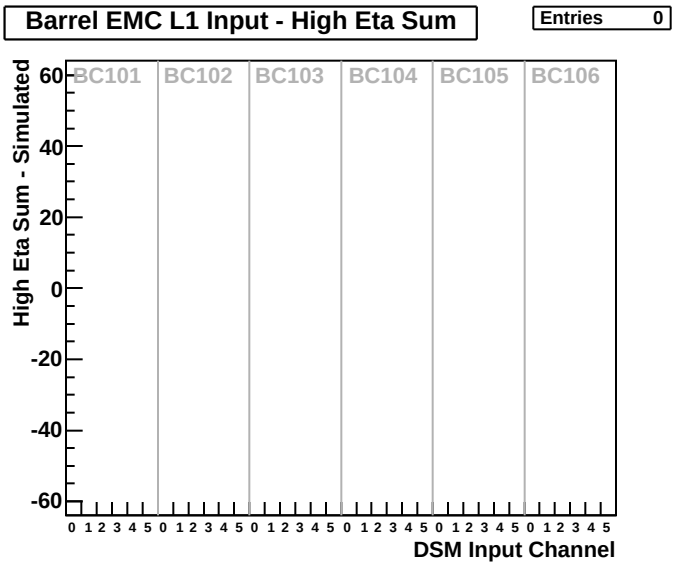

Endcap Jet Patches
Entries 18
JP ADC
JP ID

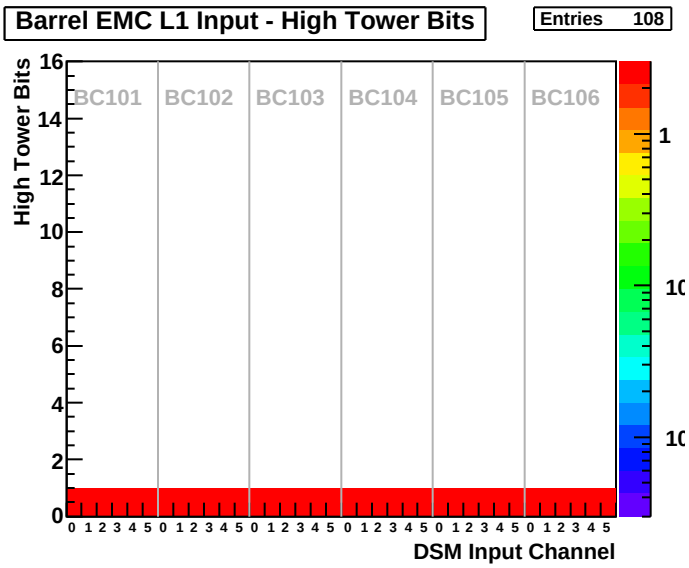

Hybrid Jet Patches
Entries 6
JP ADC
JP ID

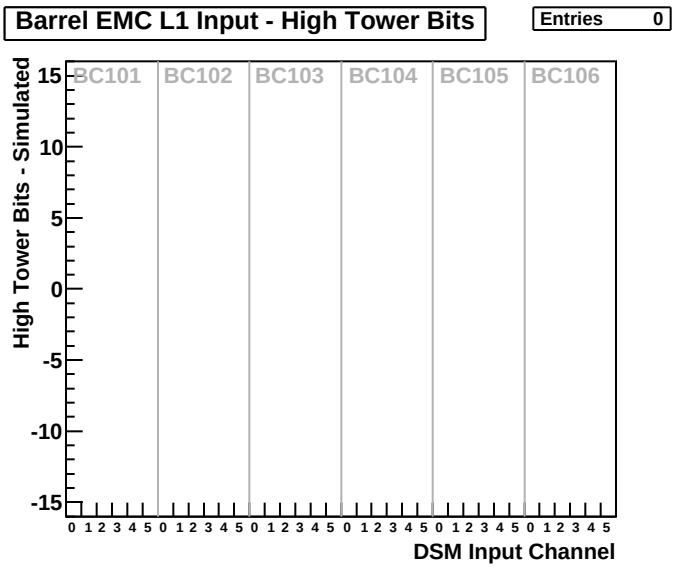

Barrel EMC L1 Input - Low Eta Sum
Entries 108
Low Eta Sum
BC101 BC102 BC103 BC104 BC105 BC106
DSM Input Channel

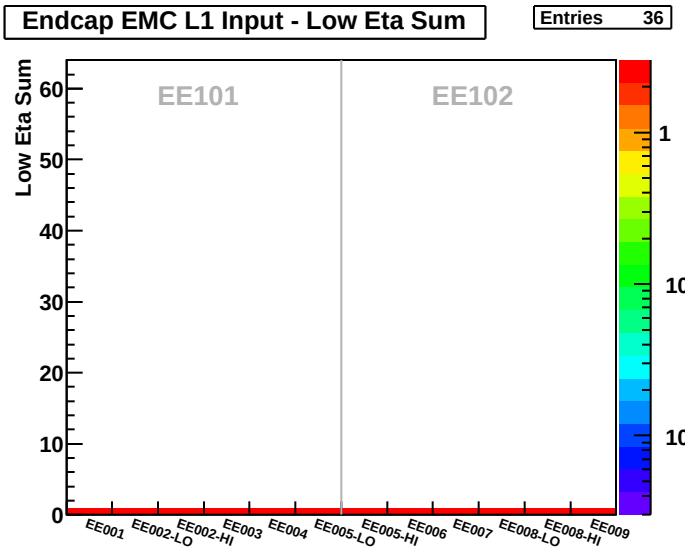

Barrel EMC L1 Input - Low Eta Sum
Entries 0
Low Eta Sum - Simulated
BC101 BC102 BC103 BC104 BC105 BC106
DSM Input Channel

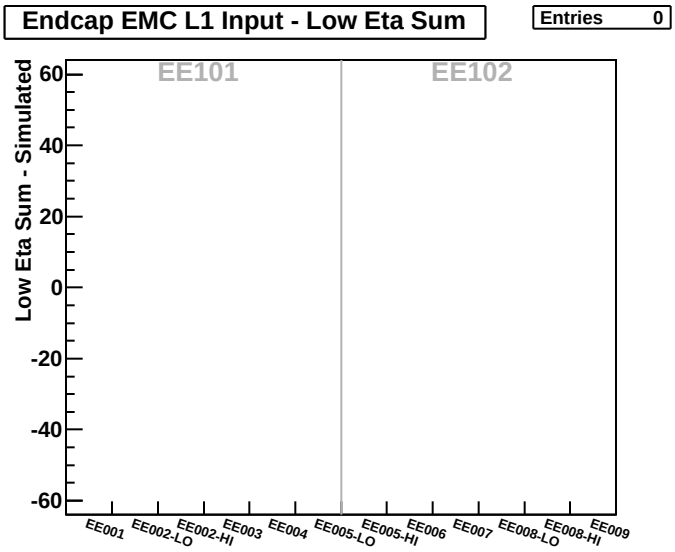

Barrel EMC L1 Input - High Eta Sum
Entries 108
High Eta Sum
BC101 BC102 BC103 BC104 BC105 BC106
DSM Input Channel

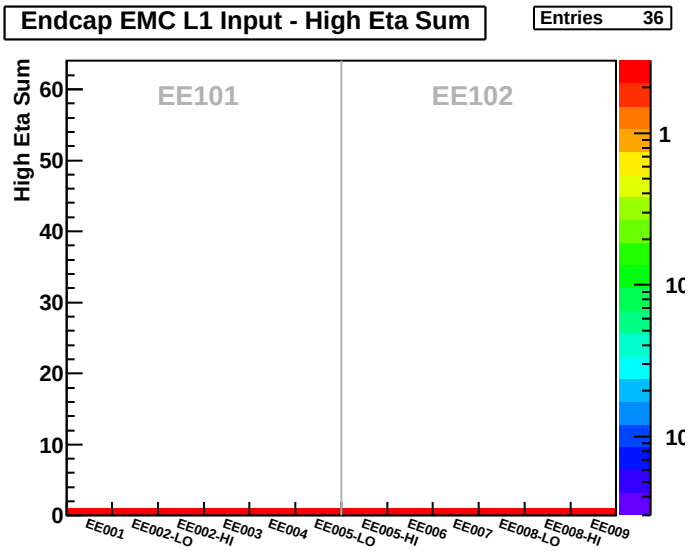

Barrel EMC L1 Input - High Eta Sum
Entries 0
High Eta Sum - Simulated
BC101 BC102 BC103 BC104 BC105 BC106
DSM Input Channel

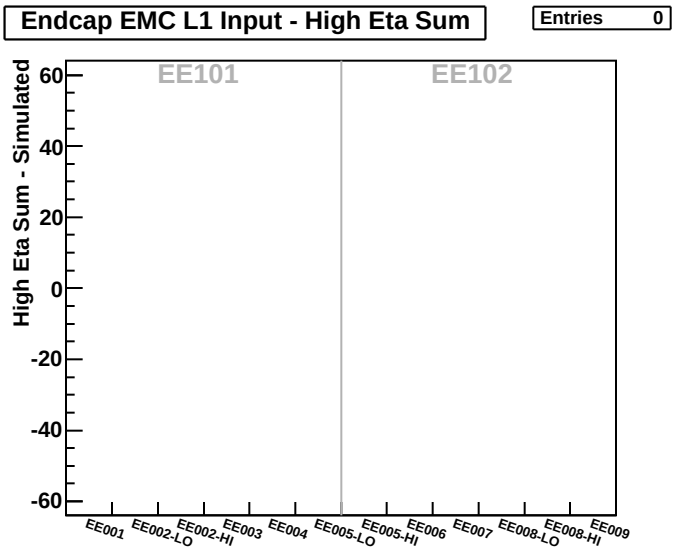

Barrel EMC L1 Input - High Tower Bits
Entries 108
High Tower Bits
BC101 BC102 BC103 BC104 BC105 BC106
DSM Input Channel

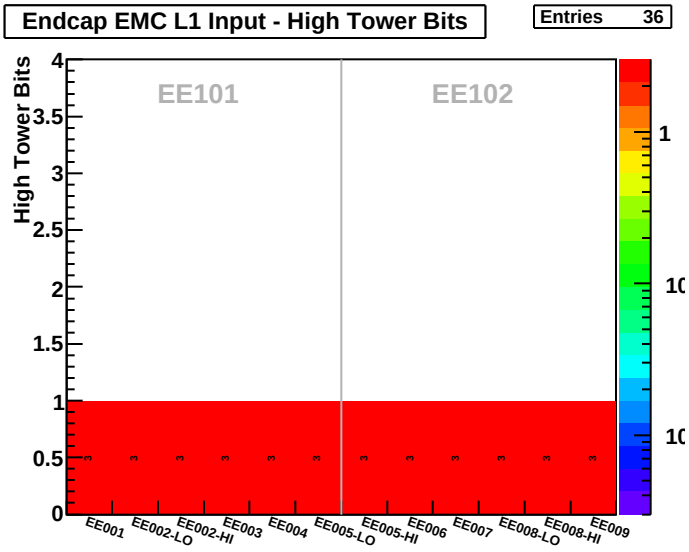

Barrel EMC L1 Input - High Tower Bits
Entries 0
High Tower Bits - Simulated
BC101 BC102 BC103 BC104 BC105 BC106
DSM Input Channel

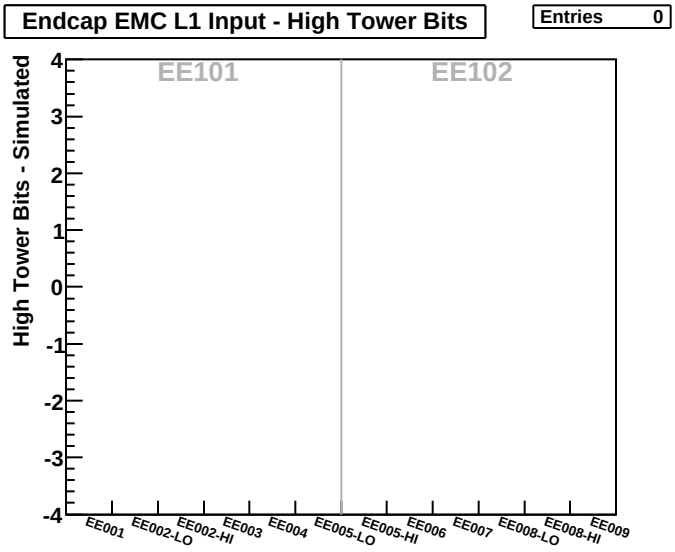

Endcap EMC L1 Input - Low Eta Sum
Entries 36
Low Eta Sum
EE101
EE102
EE001 EE002-LO EE002-HI EE003 EE004 EE005-LO EE005-HI EE006 EE007 EE008-LO EE008-HI EE009

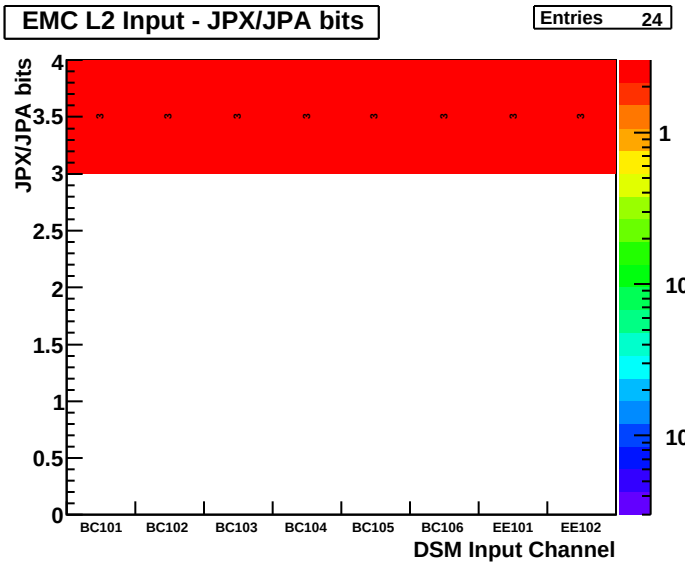

Endcap EMC L1 Input - Low Eta Sum
Entries 0
Low Eta Sum - Simulated
EE101
EE102
EE001 EE002-LO EE002-HI EE003 EE004 EE005-LO EE005-HI EE006 EE007 EE008-LO EE008-HI EE009

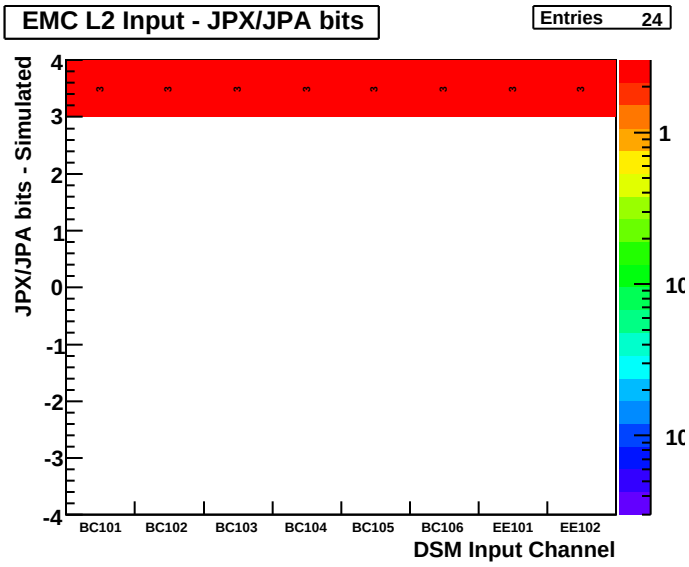

Endcap EMC L1 Input - High Eta Sum
Entries 36
High Eta Sum
EE101
EE102
EE001 EE002-LO EE002-HI EE003 EE004 EE005-LO EE005-HI EE006 EE007 EE008-LO EE008-HI EE009

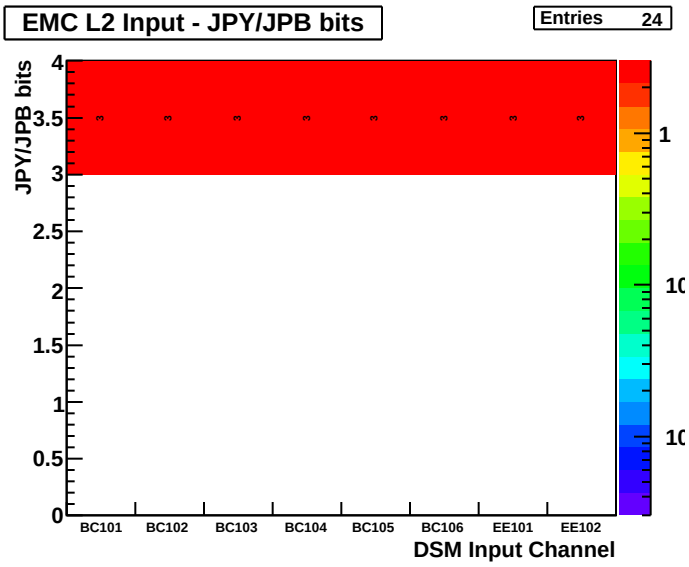

Endcap EMC L1 Input - High Eta Sum
Entries 0
High Eta Sum - Simulated
EE101
EE102
EE001 EE002-LO EE002-HI EE003 EE004 EE005-LO EE005-HI EE006 EE007 EE008-LO EE008-HI EE009

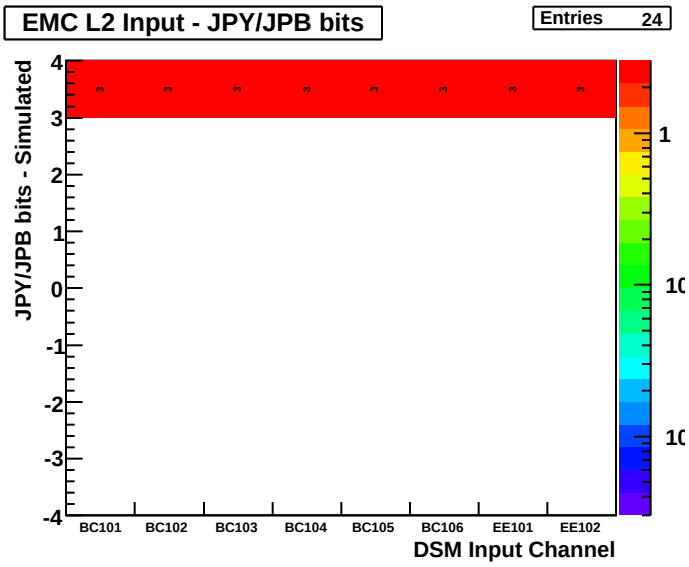

Endcap EMC L1 Input - High Tower Bits
Entries 36
High Tower Bits
EE101
EE102
EE001 EE002-LO EE002-HI EE003 EE004 EE005-LO EE005-HI EE006 EE007 EE008-LO EE008-HI EE009

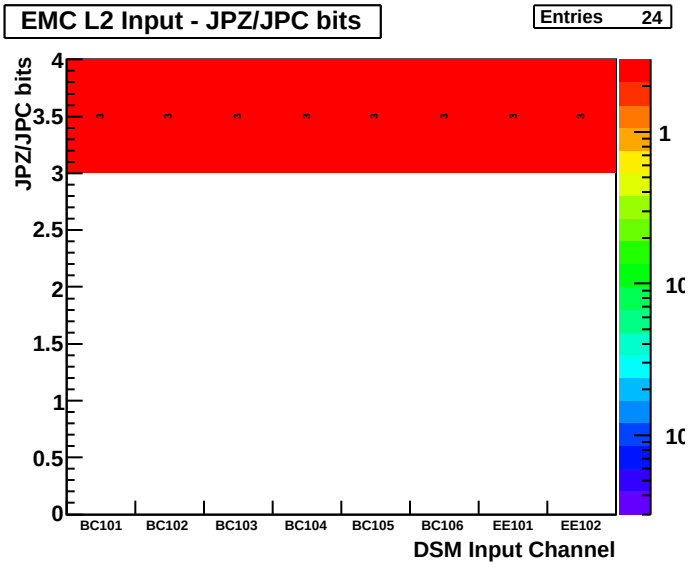

Endcap EMC L1 Input - High Tower Bits
Entries 0
High Tower Bits - Simulated
EE101
EE102
EE001 EE002-LO EE002-HI EE003 EE004 EE005-LO EE005-HI EE006 EE007 EE008-LO EE008-HI EE009

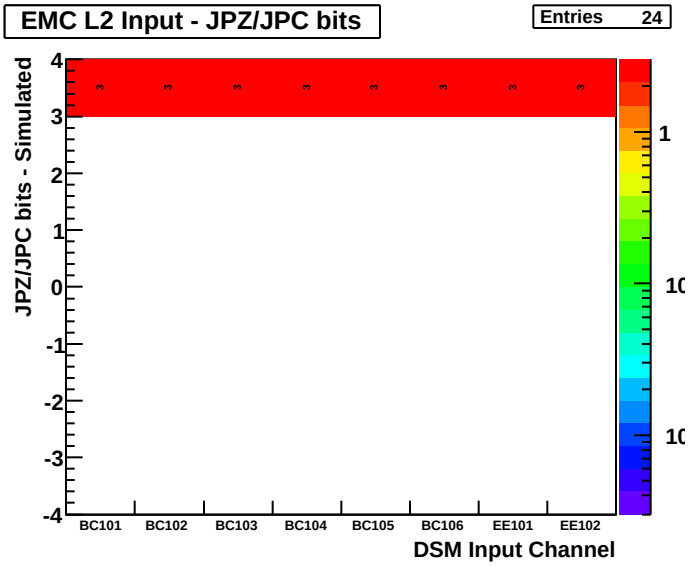

EMC L2 Input - JPX/JPA bits
Entries 24
JPX/JPA bits
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

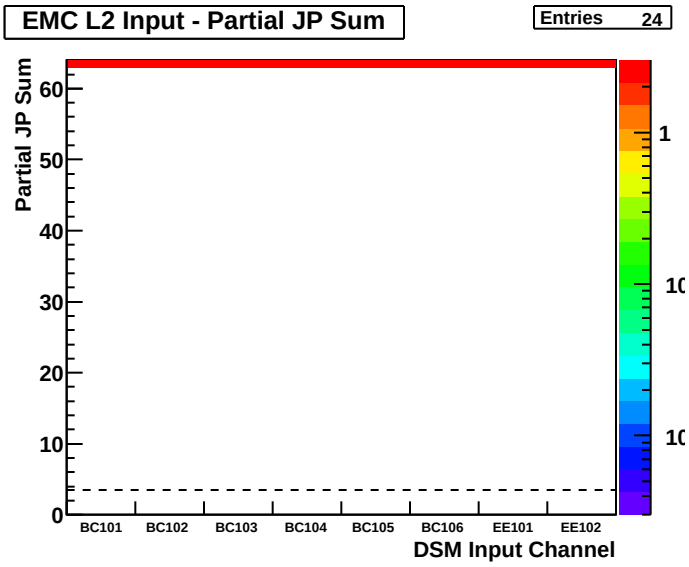

EMC L2 Input - JPX/JPA bits
Entries 24
JPX/JPA bits - Simulated
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

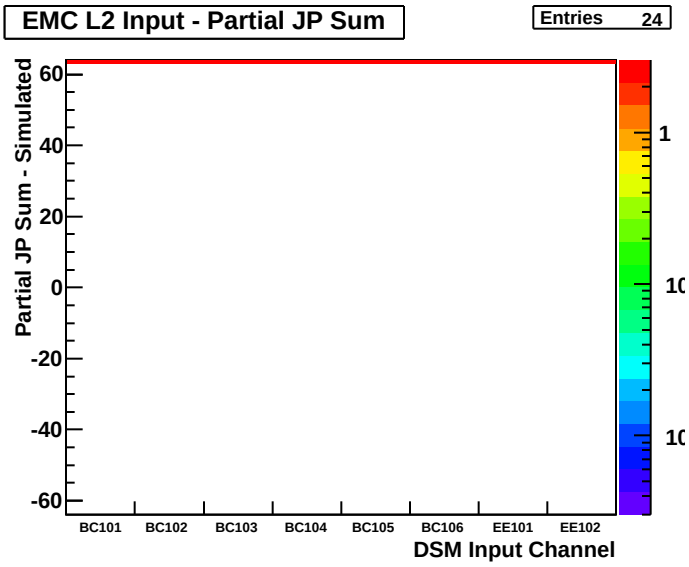

EMC L2 Input - JPY/JPB bits
Entries 24
JPY/JPB bits
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

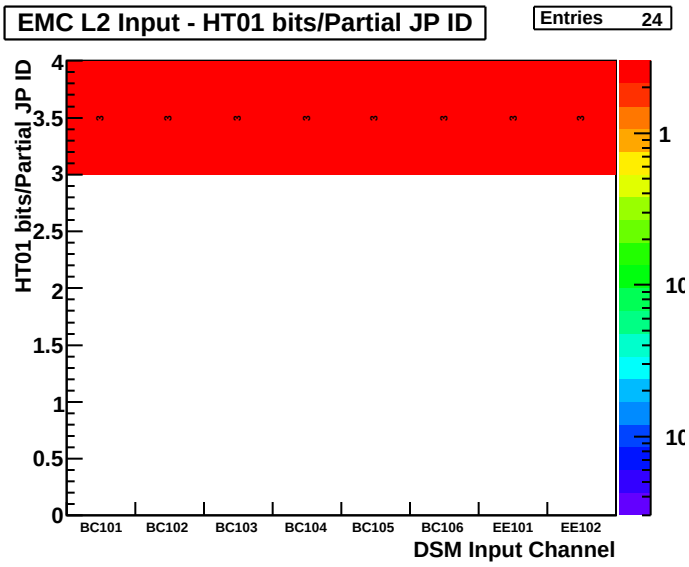

EMC L2 Input - JPY/JPB bits
Entries 24
JPY/JPB bits - Simulated
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

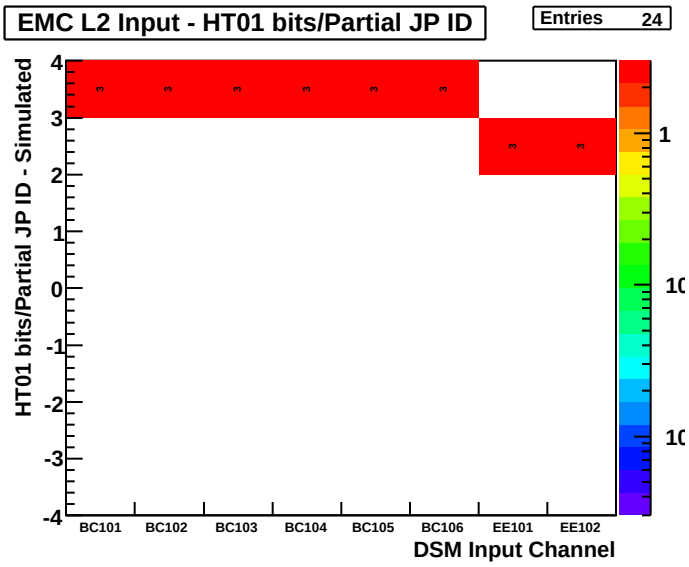

EMC L2 Input - JPZ/JPC bits
Entries 24
JPZ/JPC bits
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

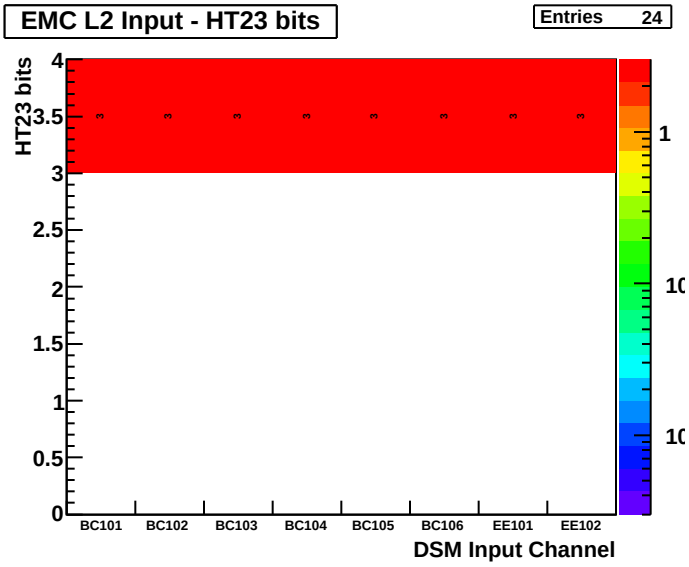

EMC L2 Input - JPZ/JPC bits
Entries 24
JPZ/JPC bits - Simulated
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

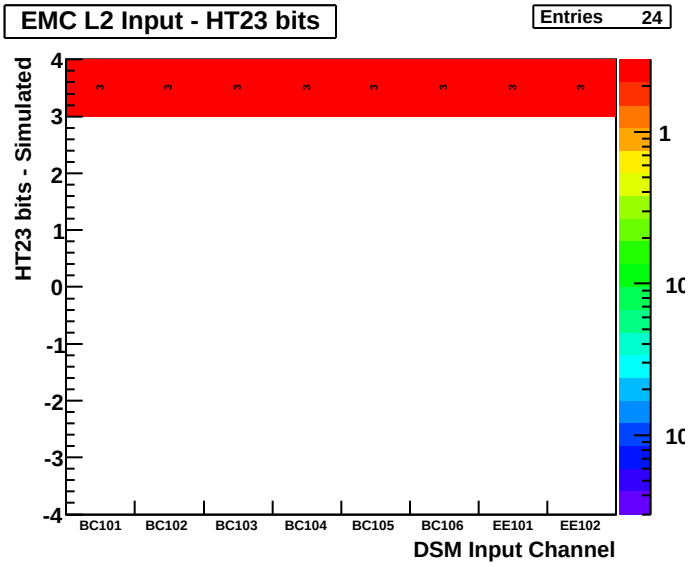

EMC L2 Input - Partial JP Sum
Entries 24
Partial JP Sum
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

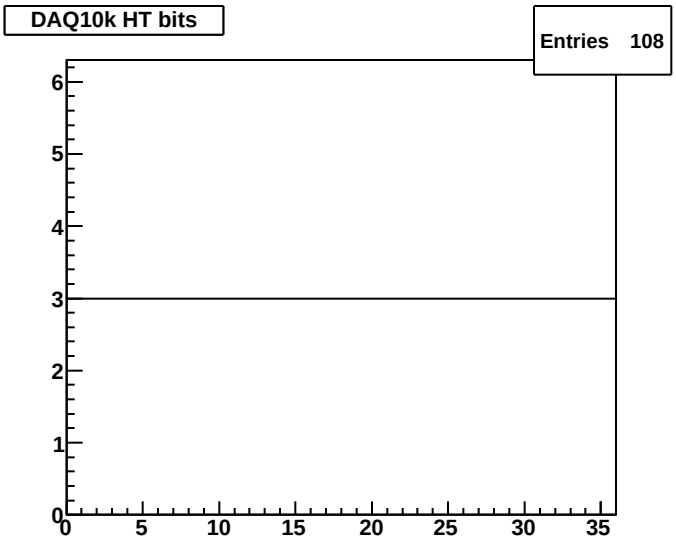

EMC L2 Input - Partial JP Sum
Entries 24
Partial JP Sum - Simulated
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

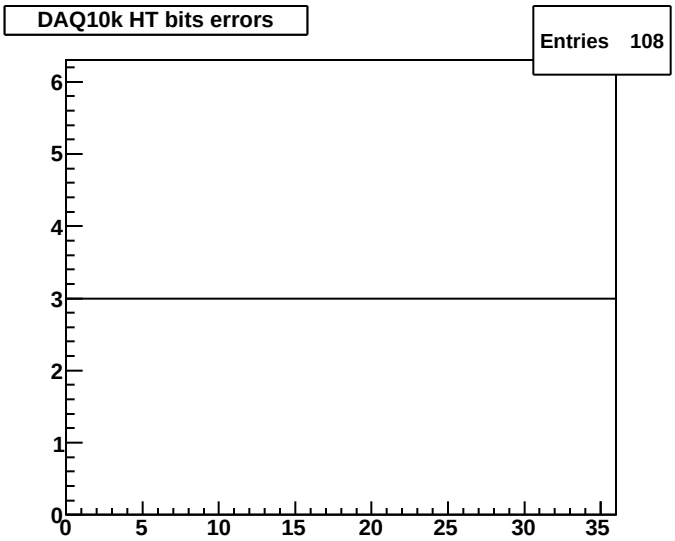

EMC L2 Input - HT01 bits/Partial JP ID
Entries 24
HT01 bits/Partial JP ID
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

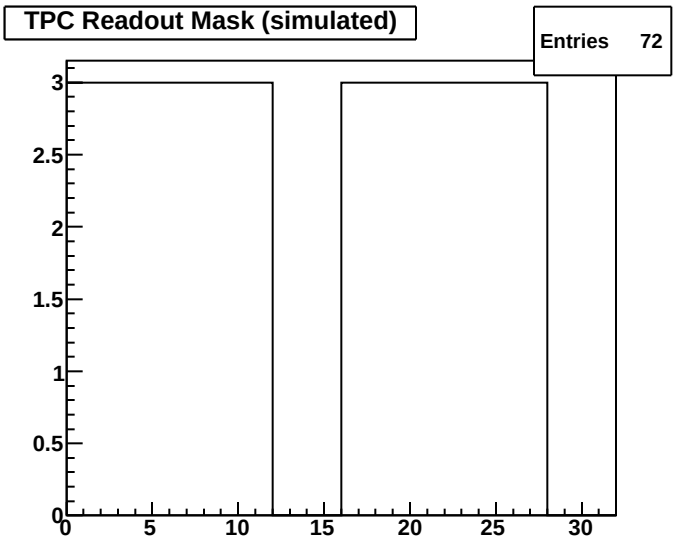

EMC L2 Input - HT01 bits/Partial JP ID
Entries 24
HT01 bits/Partial JP ID - Simulated
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

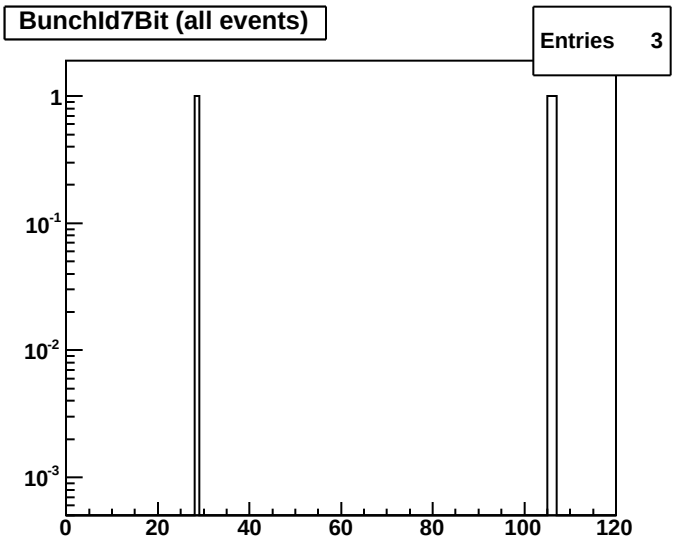

EMC L2 Input - HT23 bits
Entries 24
HT23 bits
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

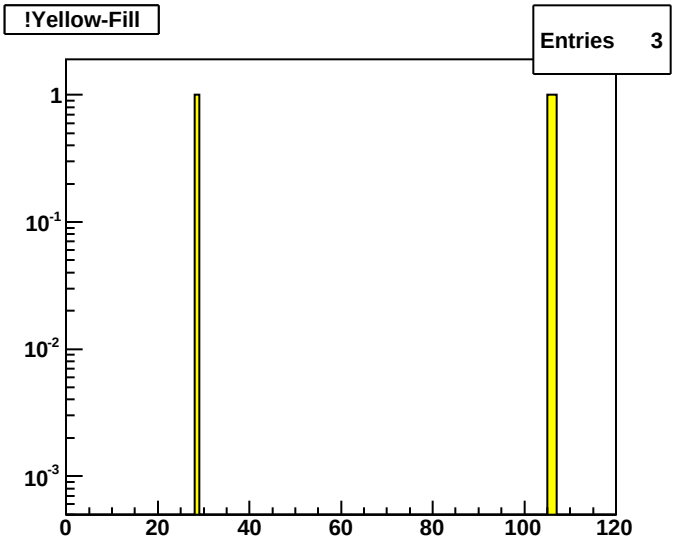

EMC L2 Input - HT23 bits
Entries 24
HT23 bits - Simulated
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

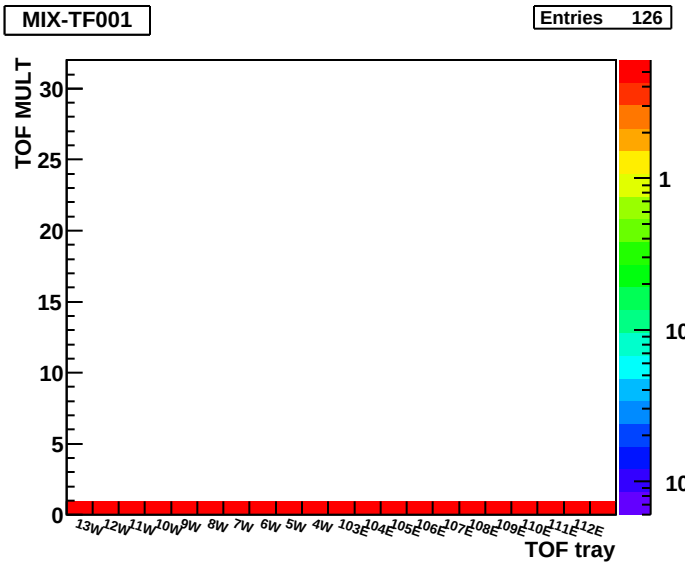

DAQ10k HT bits
Entries 108
0
1
2
3
4
5
6
0
5
10
15
20
25
30
35

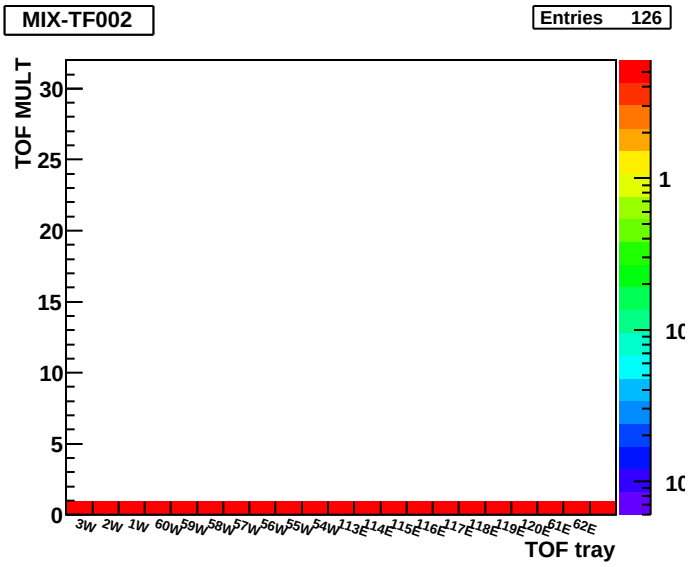

DAQ10k HT bits errors
Entries 108
0
1
2
3
4
5
6
0
5
10
15
20
25
30
35

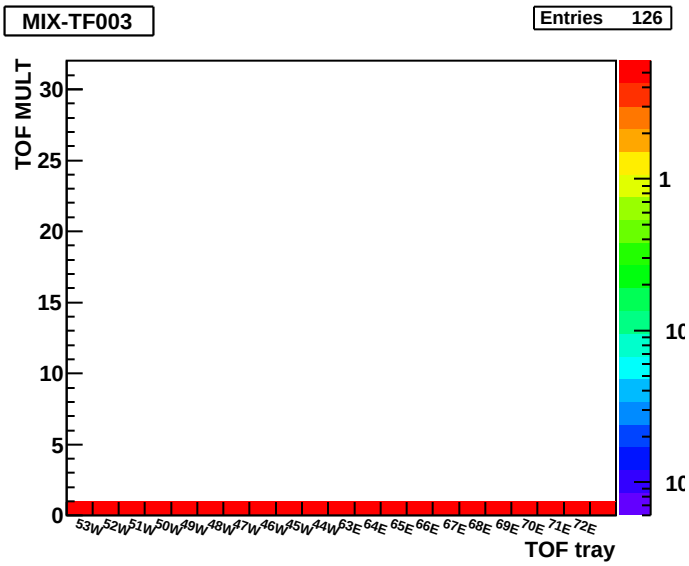

TPC Readout Mask (simulated)
Entries 72
0
0.5
1
1.5
2
2.5
3
0
5
10
15
20
25
30

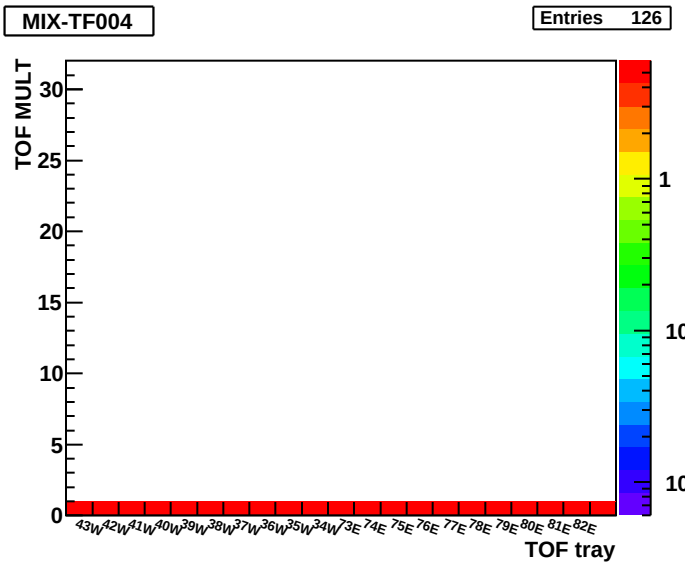

BunchId7Bit (all events)
Entries 3
1
10-1
10-2
10-3
0
20
40
60
80
100
120

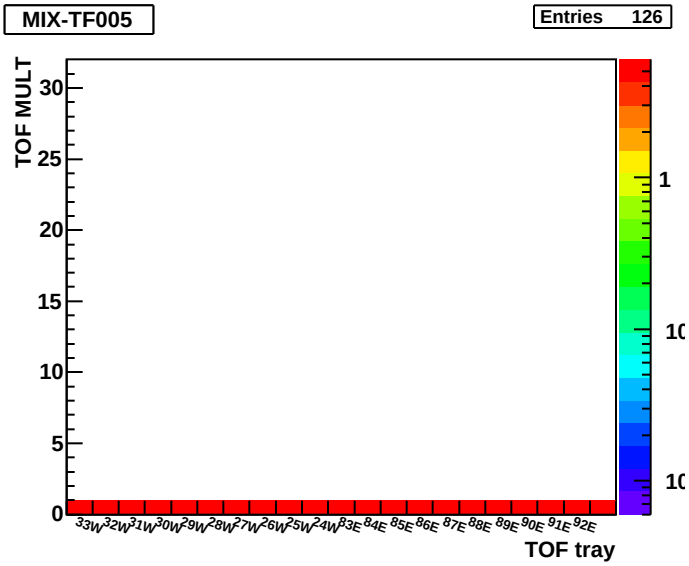

!Yellow-Fill
Entries 3
1
10-1
10-2
10-3
0
20
40
60
80
100
120

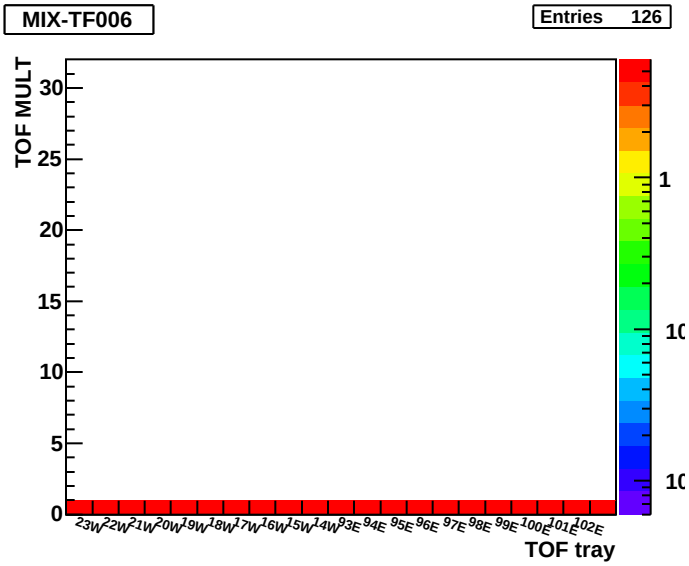

MIX-TF001
Entries 126
TOF MULT
TOF tray

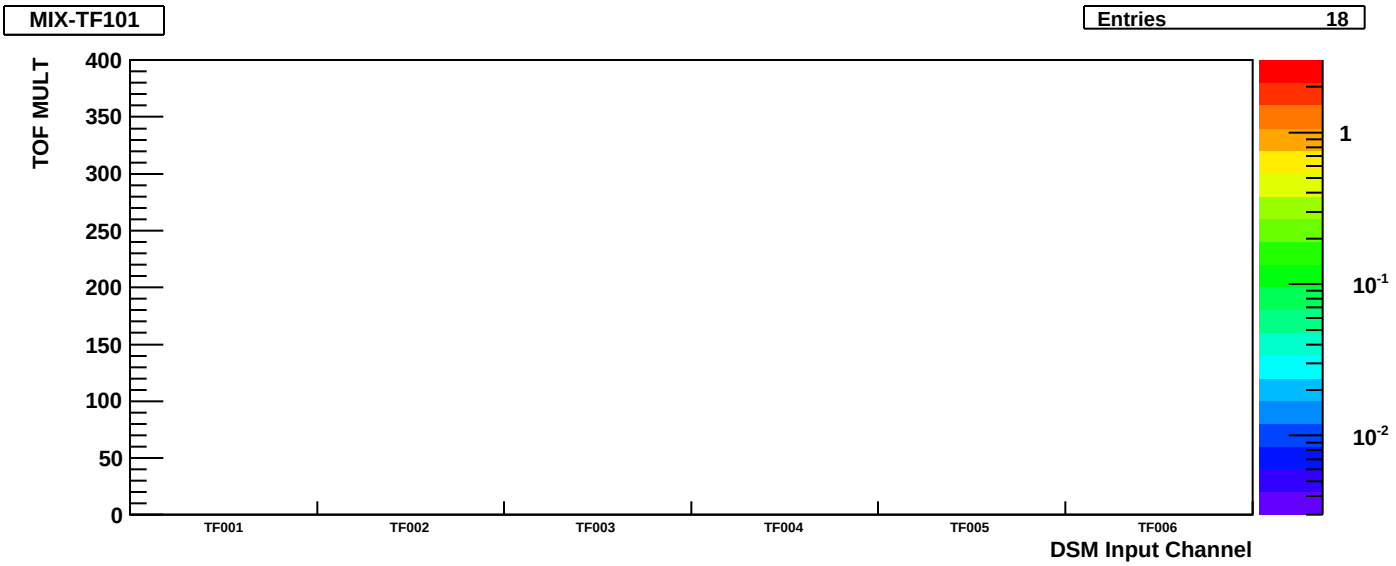

MIX-TF002
Entries 126
TOF MULT
TOF tray

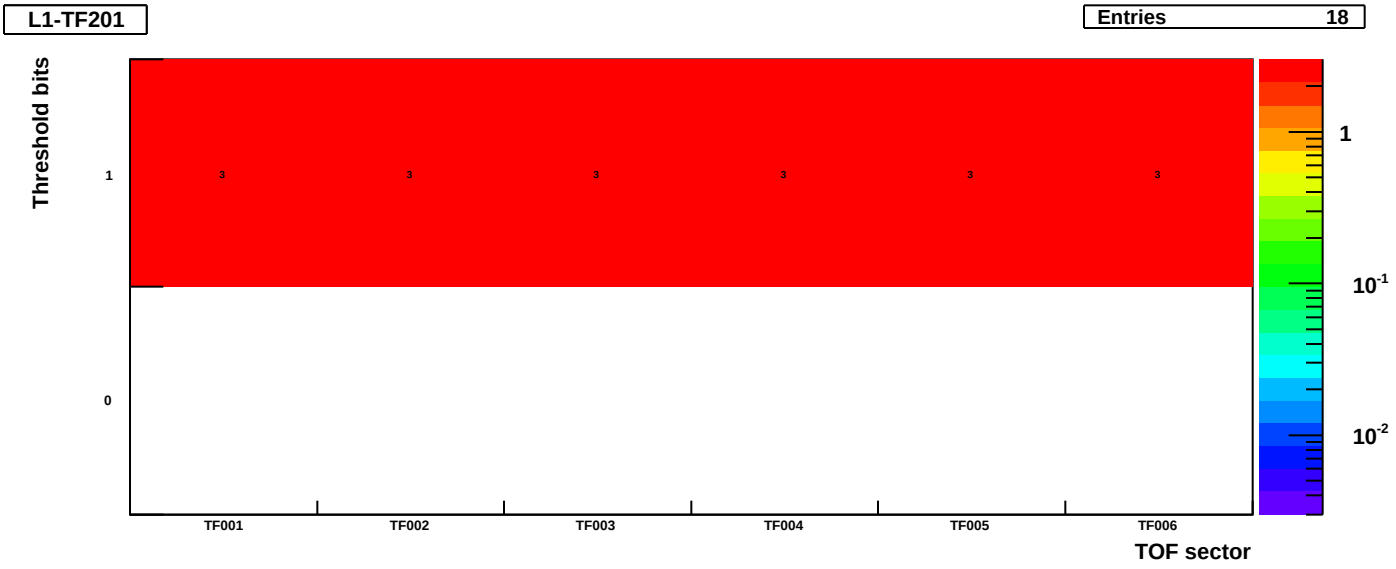

MIX-TF003
Entries 126
TOF MULT
TOF tray

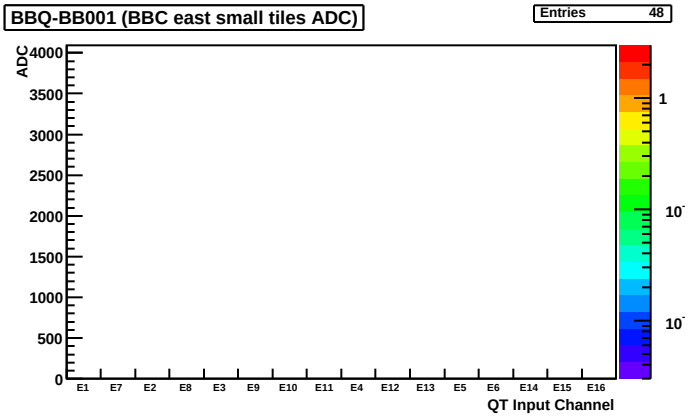

MIX-TF004
Entries 126
TOF MULT
TOF tray

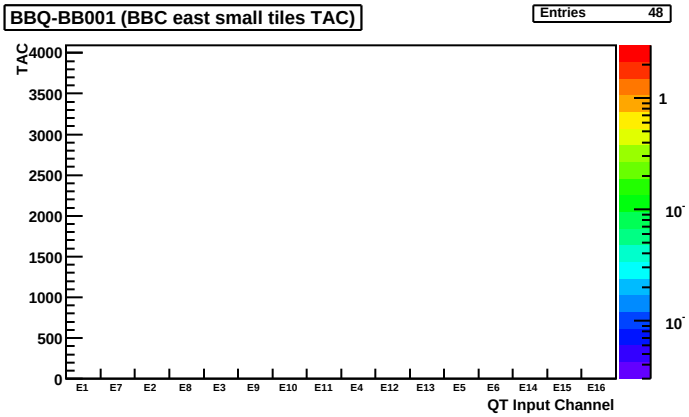

MIX-TF005
Entries 126
TOF MULT
TOF tray

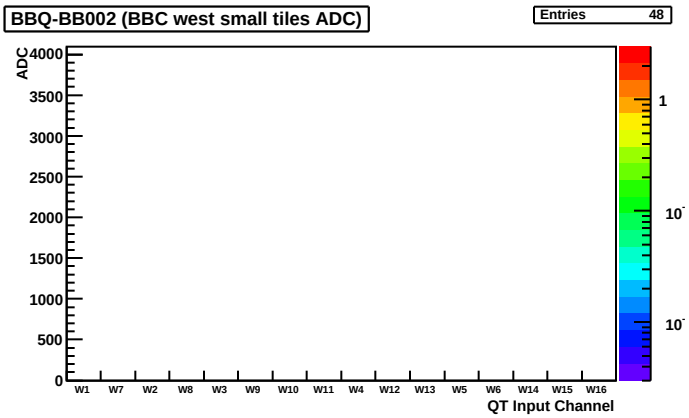

MIX-TF006
Entries 126
TOF MULT
TOF tray

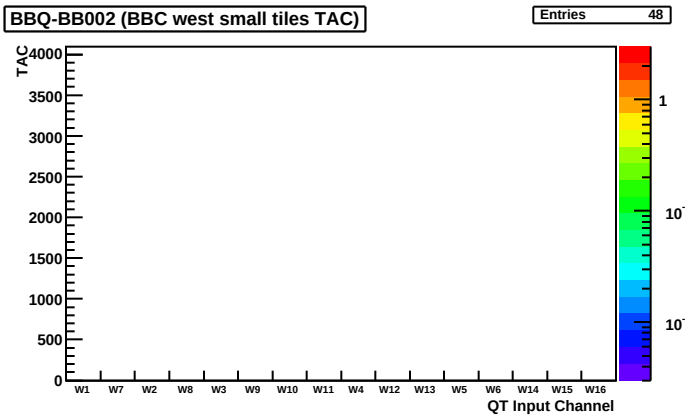

MIX-TF101
Entries 18
TOF MULT
400
350
300
250
200
150
100
50
0
TF001
TF002
TF003
TF004
TF005
TF006
DSM Input Channel
1
10-1
10-2

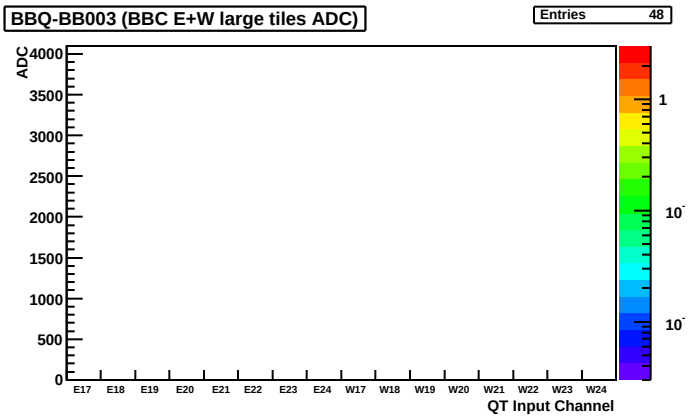

L1-TF201
Entries 18
Threshold bits
1
0
3
TF001
TF002
TF003
TF004
TF005
TF006
TOF sector
1
10-1
10-2

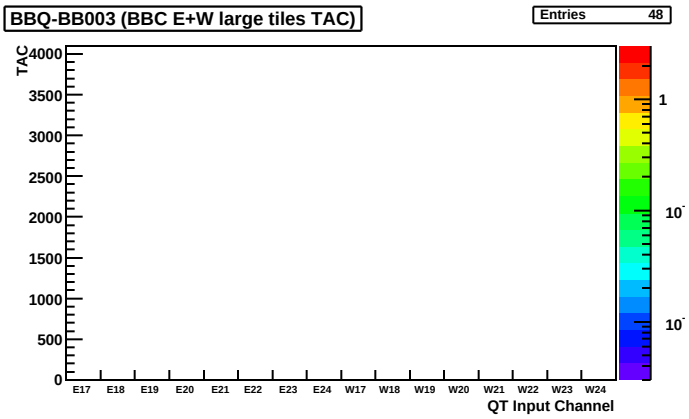

BBQ-BB001 (BBC east small tiles ADC)
Entries 48
ADC
QT Input Channel

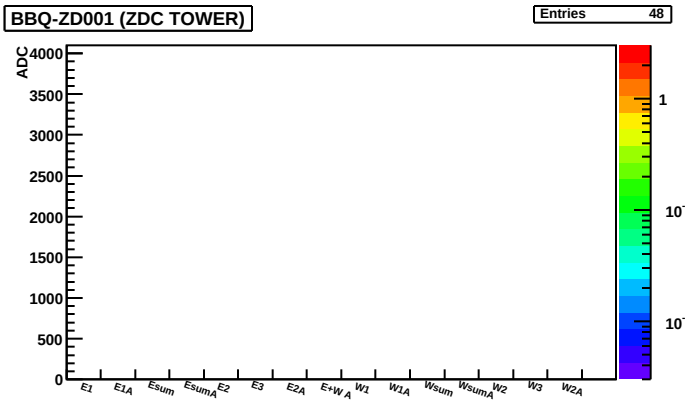

BBQ-BB001 (BBC east small tiles TAC)
Entries 48
TAC
QT Input Channel

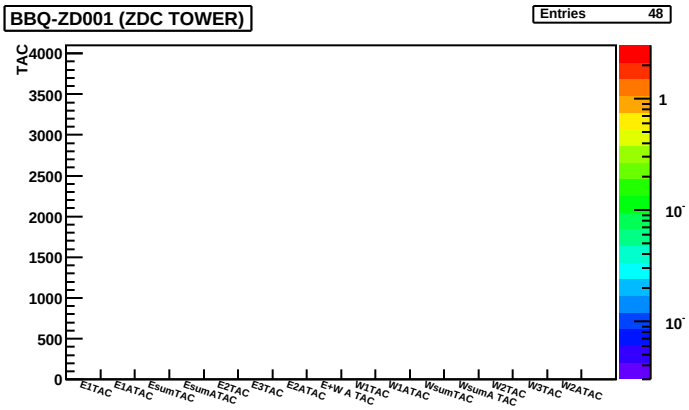

BBQ-BB002 (BBC west small tiles ADC)
Entries 48
ADC
QT Input Channel

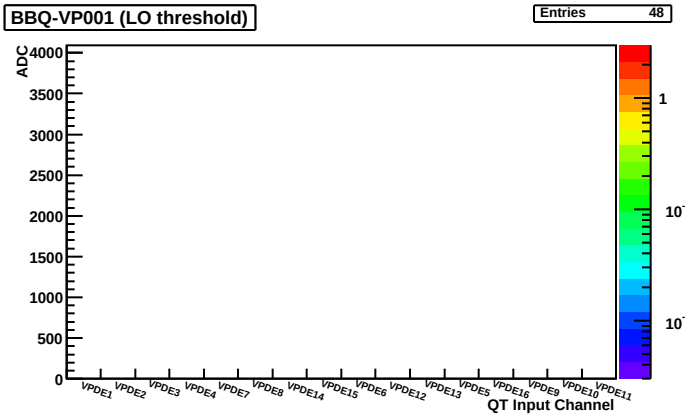

BBQ-BB002 (BBC west small tiles TAC)
Entries 48
TAC
QT Input Channel

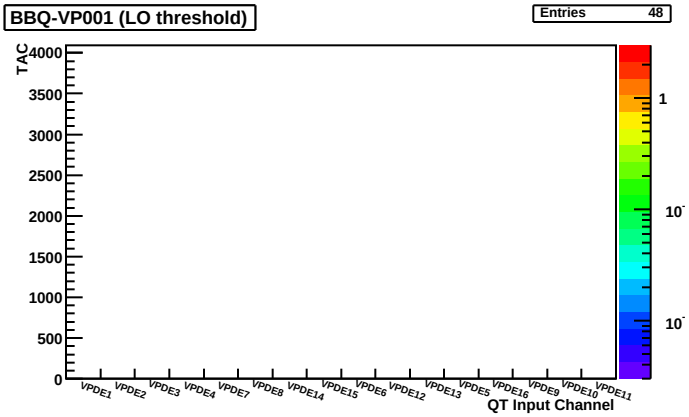

BBQ-BB003 (BBC E+W large tiles ADC)
Entries 48
ADC
QT Input Channel

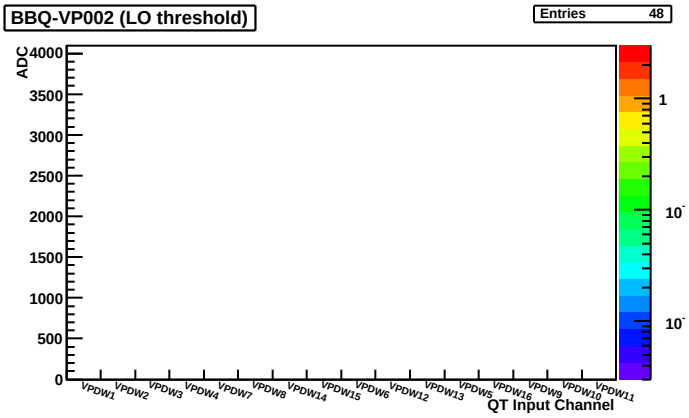

BBQ-BB003 (BBC E+W large tiles TAC)
Entries 48
TAC
QT Input Channel

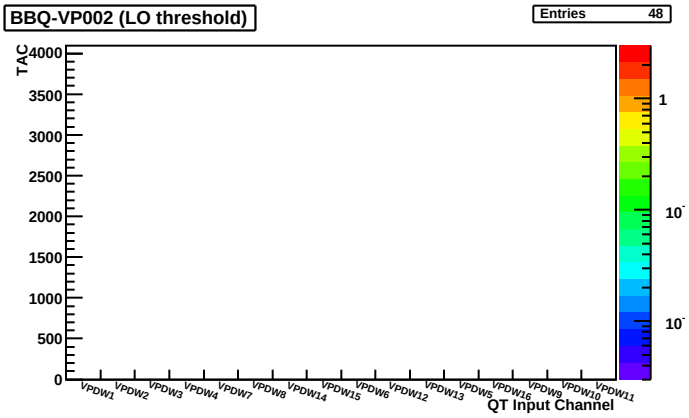

BBQ-ZD001 (ZDC TOWER)
Entries 48
ADC

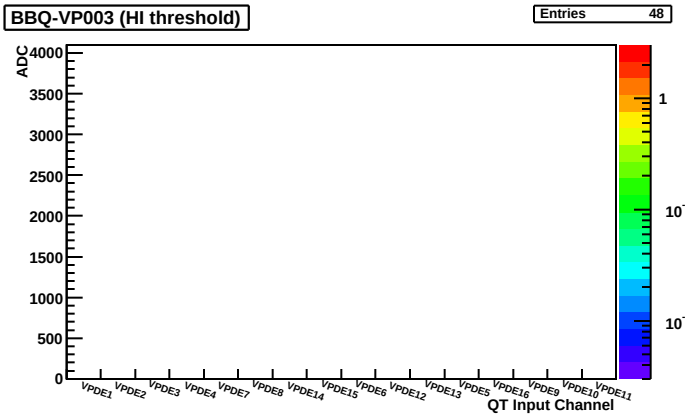

BBQ-ZD001 (ZDC TOWER)
Entries 48
TAC

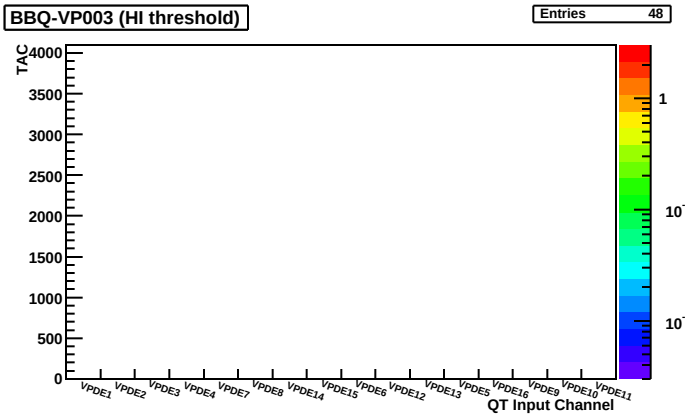

BBQ-VP001 (LO threshold)
Entries 48
ADC
QT Input Channel

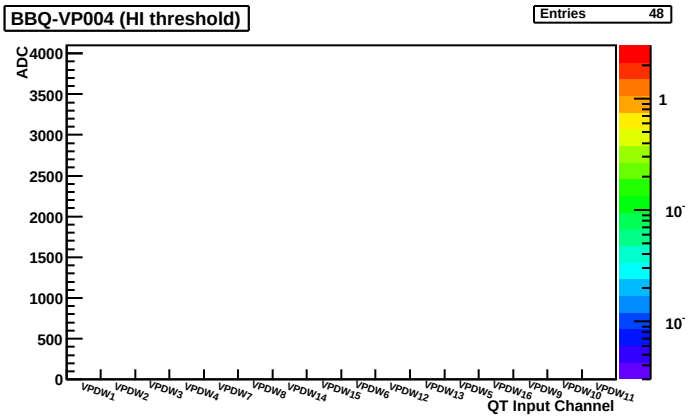

BBQ-VP001 (LO threshold)
Entries 48
TAC
QT Input Channel

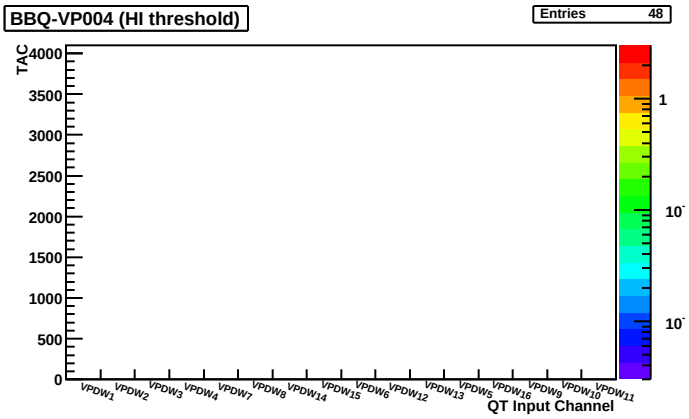

BBQ-VP002 (LO threshold)
Entries 48
ADC
QT Input Channel

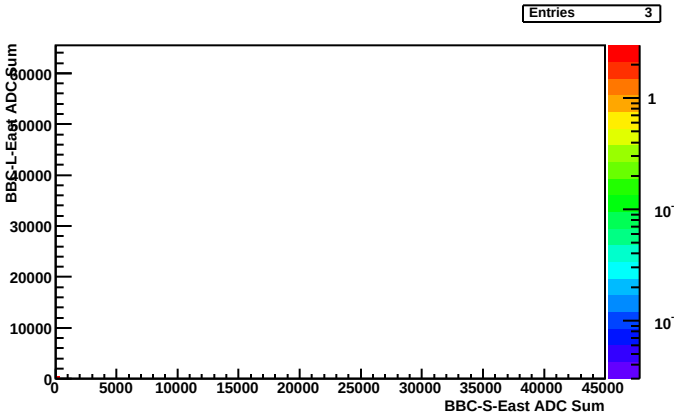

BBQ-VP002 (LO threshold)
Entries 48
TAC
QT Input Channel

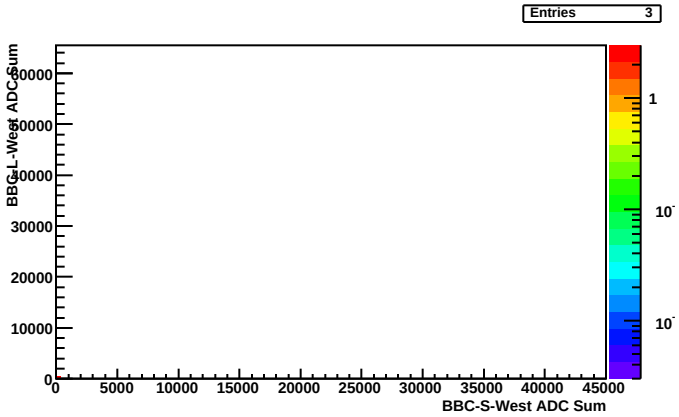

BBQ-VP003 (HI threshold)
Entries 48
ADC
QT Input Channel

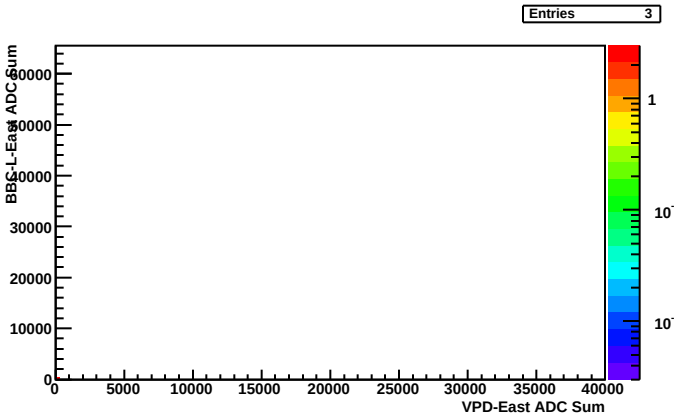

BBQ-VP003 (HI threshold)
Entries 48
TAC
QT Input Channel

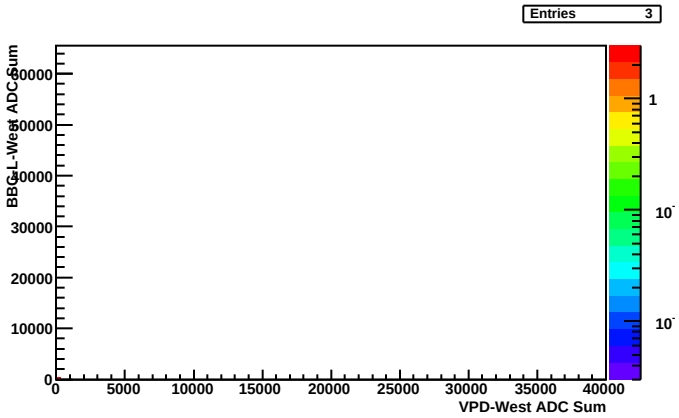

BBQ-VP004 (HI threshold)
Entries 48
ADC
QT Input Channel

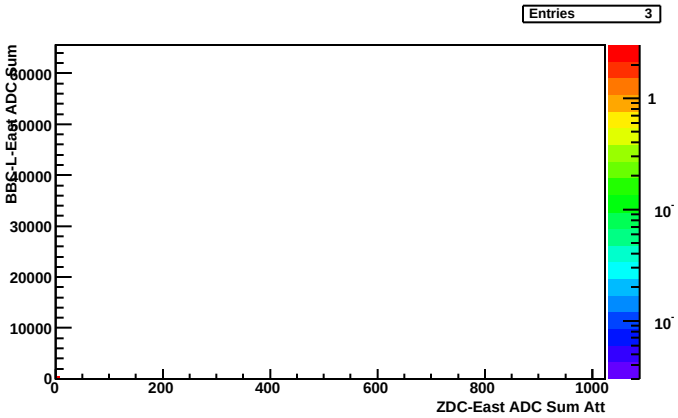

BBQ-VP004 (HI threshold)
Entries 48
TAC
QT Input Channel

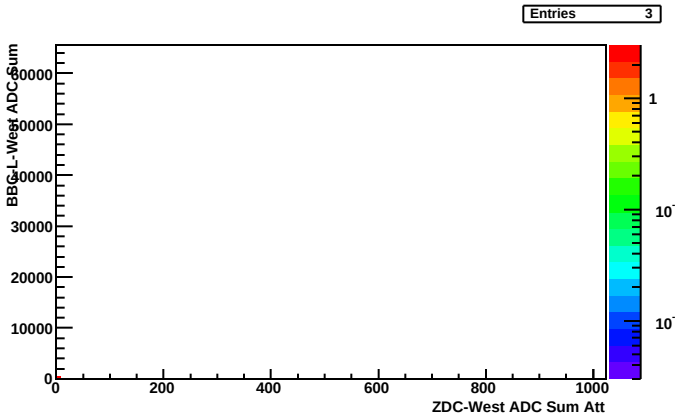

Entries 3
BBC-L-East ADC Sum
BBC-S-East ADC Sum

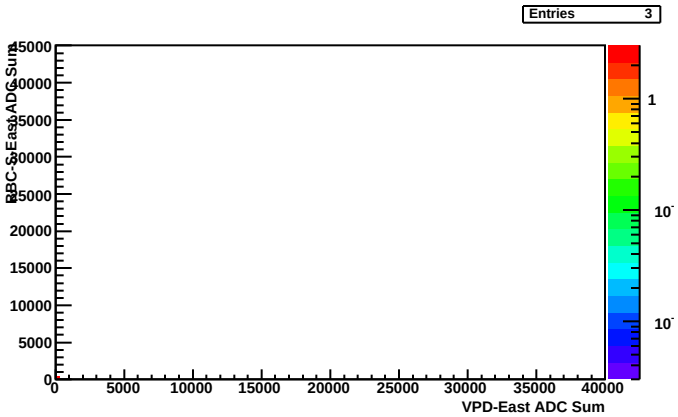

Entries 3
BBC-L-West ADC Sum
BBC-S-West ADC Sum

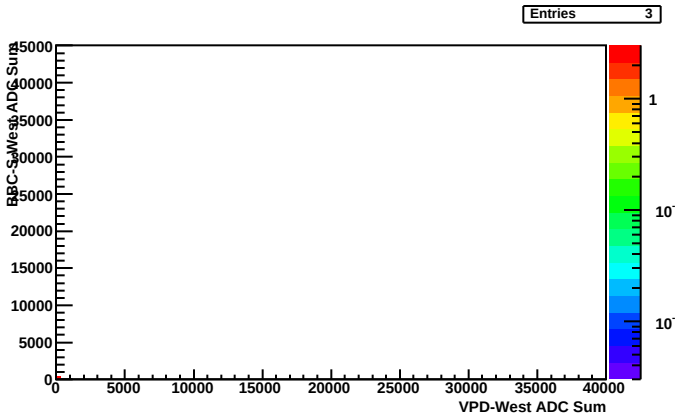

Entries 3
BBC-L-East ADC Sum
VPD-East ADC Sum

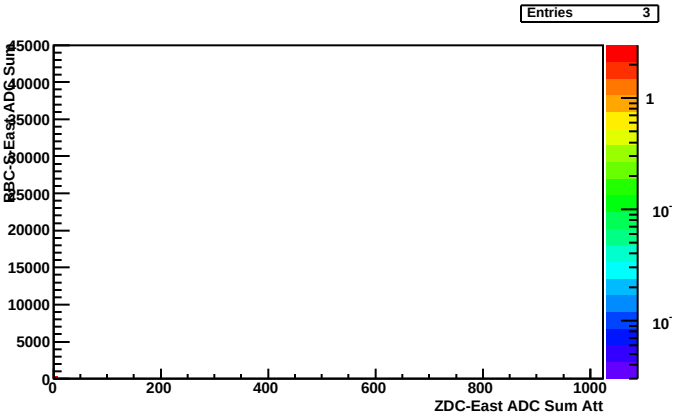

Entries 3
BBC-L-West ADC Sum
VPD-West ADC Sum

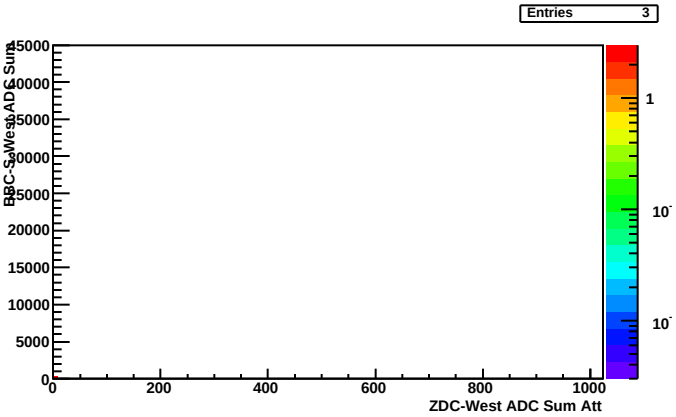

Entries 3
BBC-L-East ADC Sum
ZDC-East ADC Sum Att

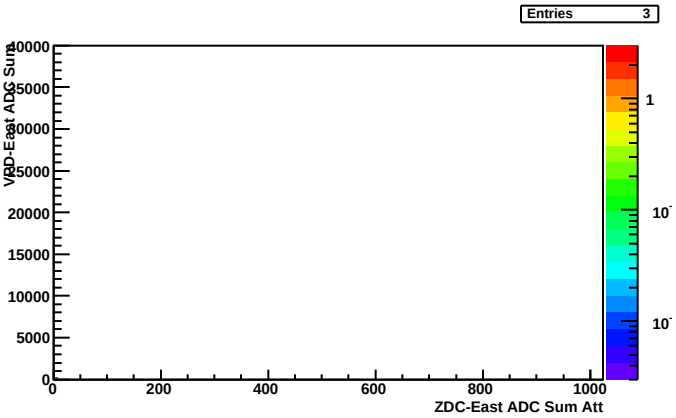

Entries 3
BBC-L-West ADC Sum
ZDC-West ADC Sum Att

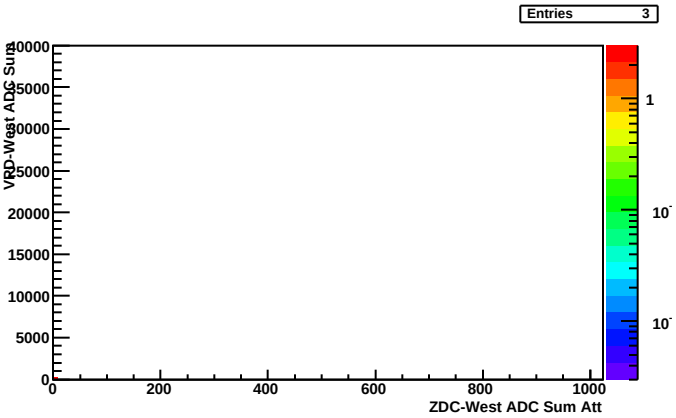

Entries 3
BBC-S-East ADC Sum
VPD-East ADC Sum

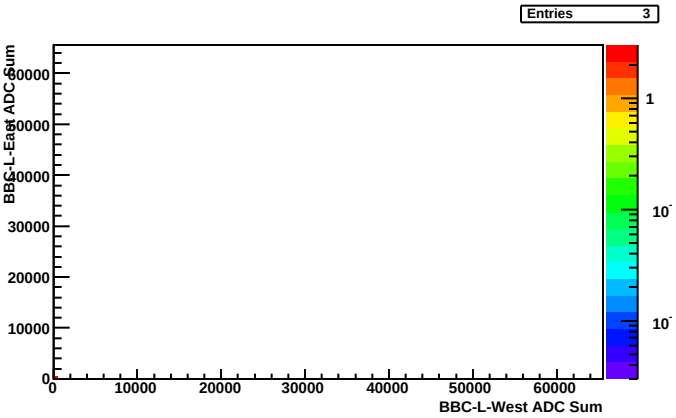

Entries 3
BBC-S-West ADC Sum
VPD-West ADC Sum

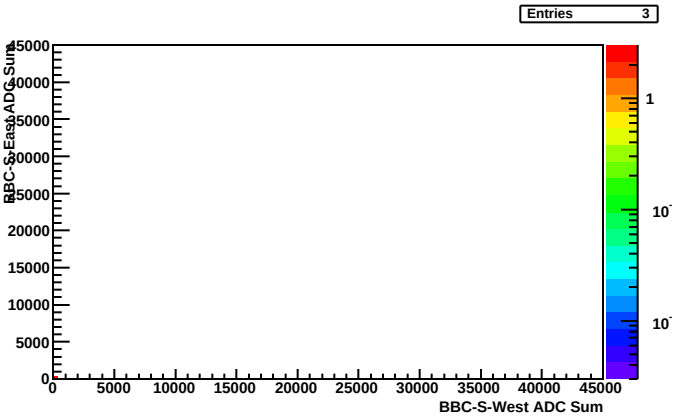

Entries 3
BBC-S-East ADC Sum
ZDC-East ADC Sum Att

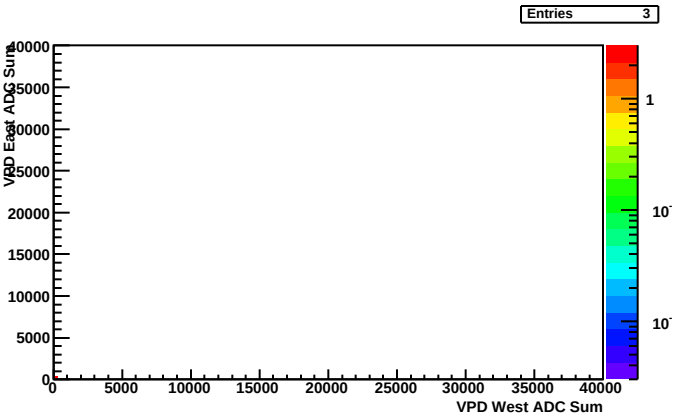

Entries 3
BBC-S-West ADC Sum
ZDC-West ADC Sum Att

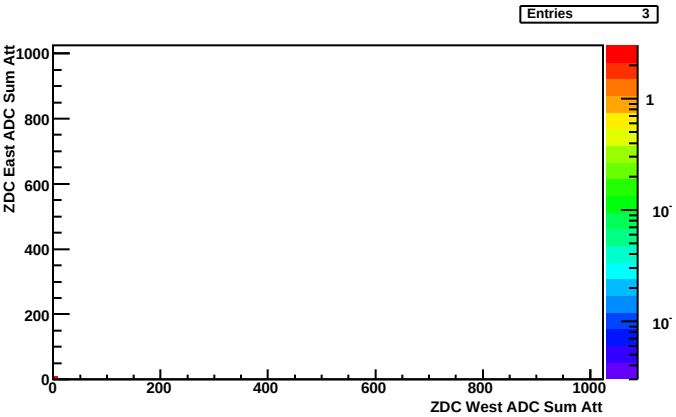

Entries 3
VPD-East ADC Sum
ZDC-East ADC Sum Att

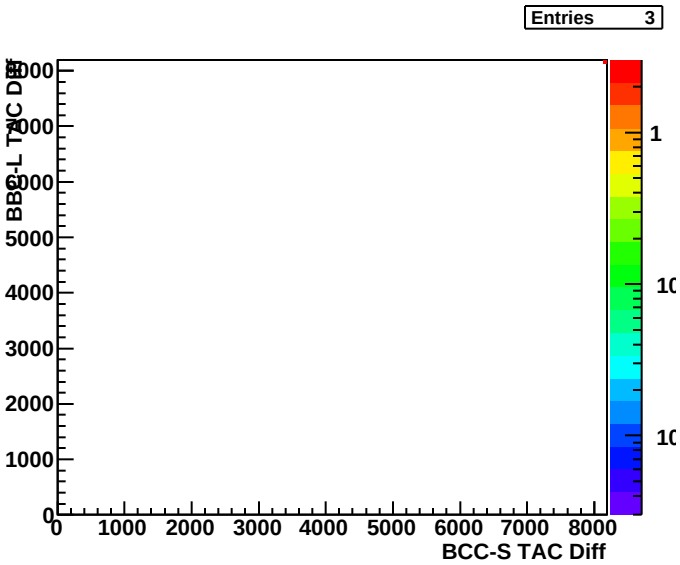

Entries 3
VPD-West ADC Sum
ZDC-West ADC Sum Att

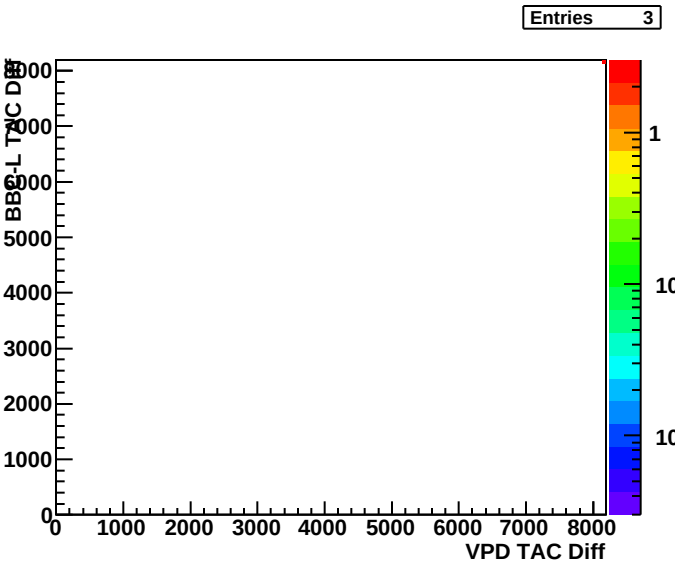

Entries 3
BBC-L-East ADC Sum
BBC-L-West ADC Sum

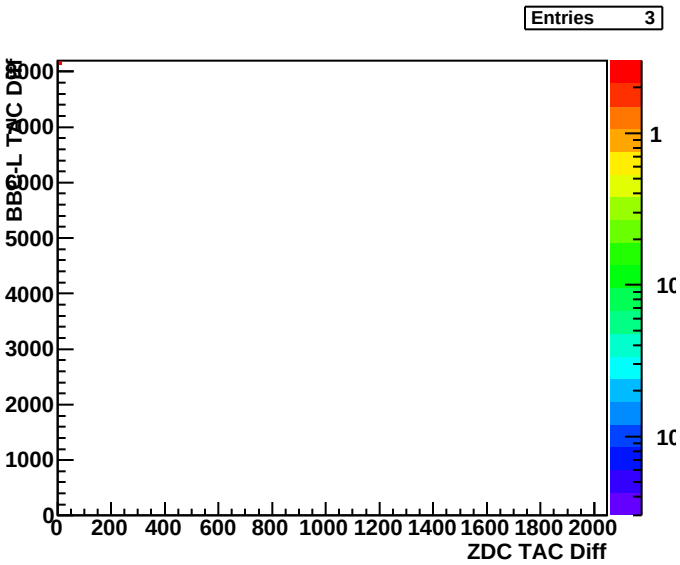

Entries 3
BBC-S-East ADC Sum
BBC-S-West ADC Sum

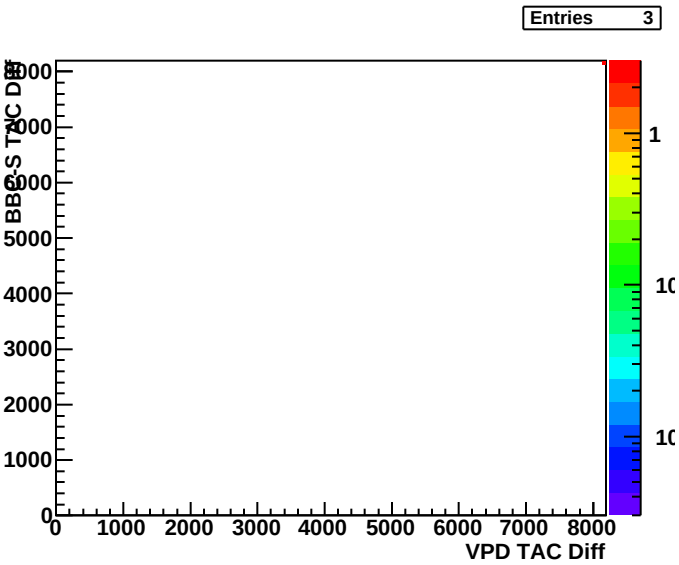

Entries 3
VPD East ADC Sum
VPD West ADC Sum

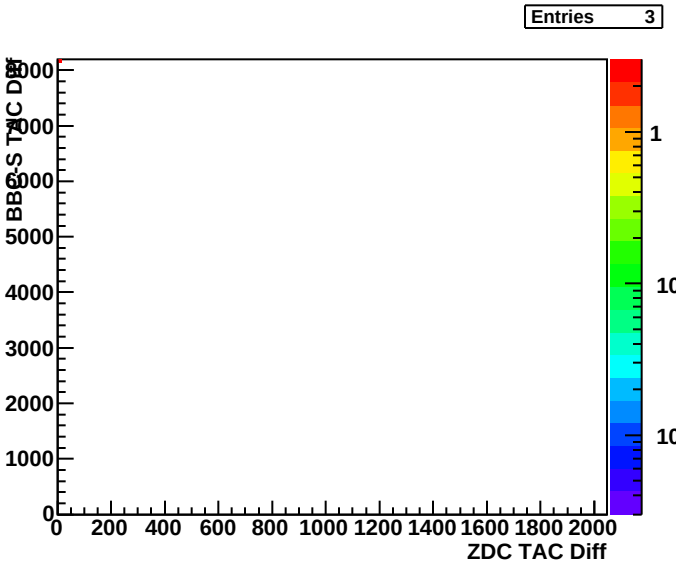

Entries 3
ZDC East ADC Sum Att
ZDC West ADC Sum Att

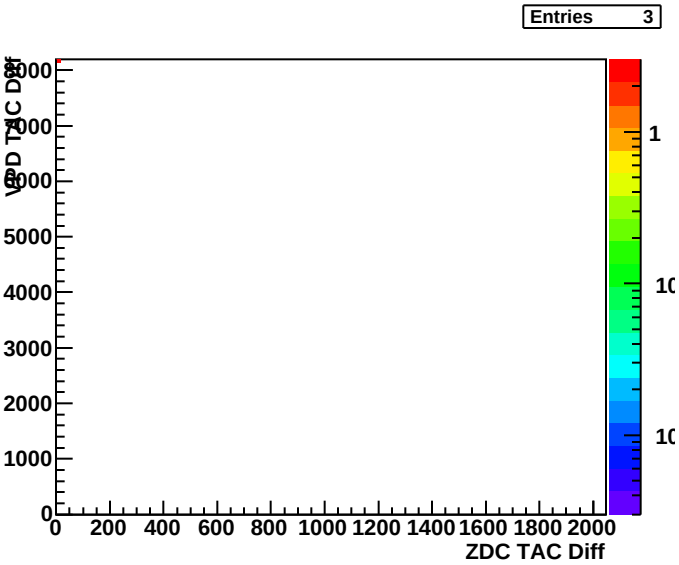

Entries 3
BBC-L TAC Diff
BCC-S TAC Diff

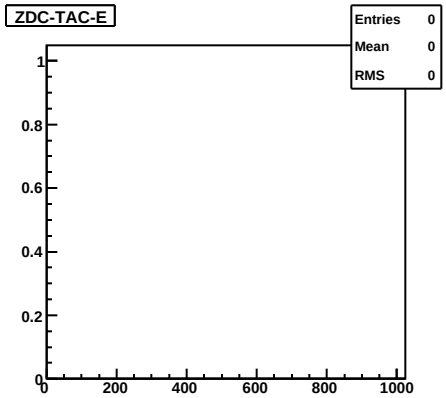

Entries 3
BBC-L TAC Diff
VPD TAC Diff

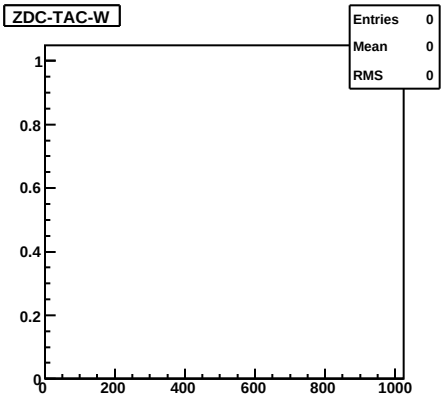

Entries 3
BBC-L TAC Diff
ZDC TAC Diff

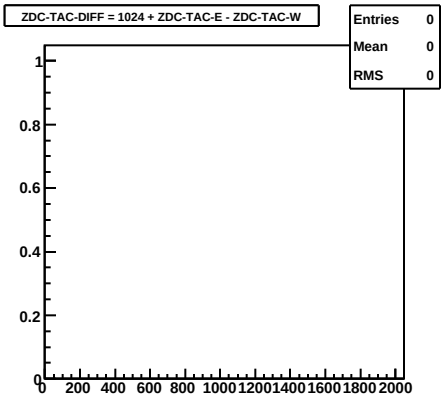

Entries 3
BBC-S TAC Diff
VPD TAC Diff

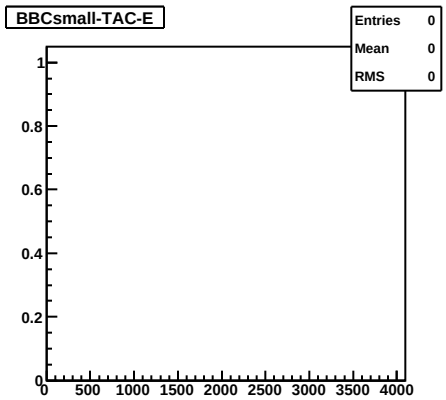

Entries 3
BBC-S TAC Diff
ZDC TAC Diff

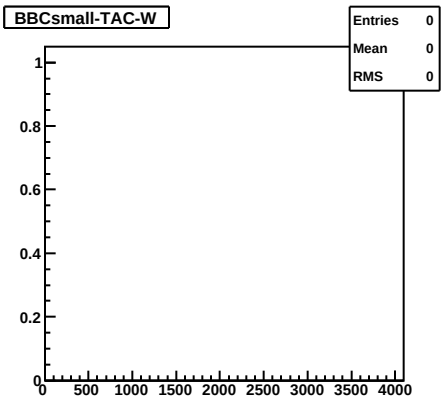

Entries 3
VPD TAC Diff
ZDC TAC Diff

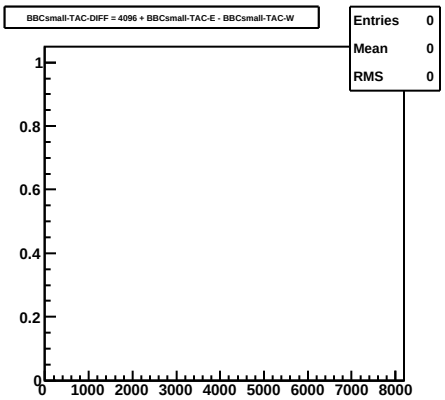

ZDC-TAC-E
Entries 0
Mean 0
RMS 0

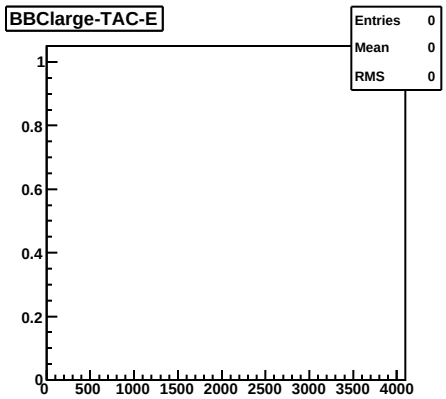

ZDC-TAC-W
Entries 0
Mean 0
RMS 0

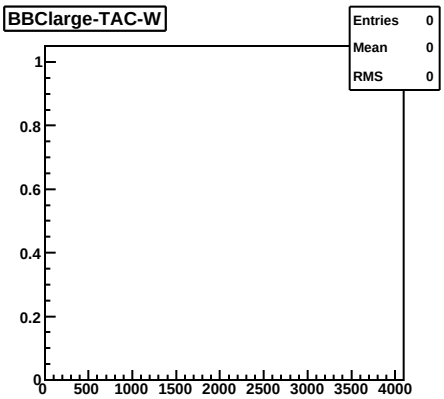

ZDC-TAC-DIFF = 1024 + ZDC-TAC-E - ZDC-TAC-W
Entries 0
Mean 0
RMS 0

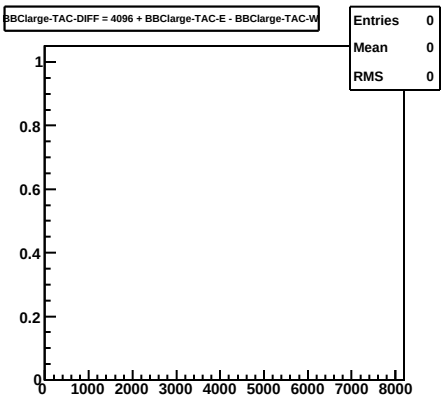

BBCsmall-TAC-E
Entries 0
Mean 0
RMS 0

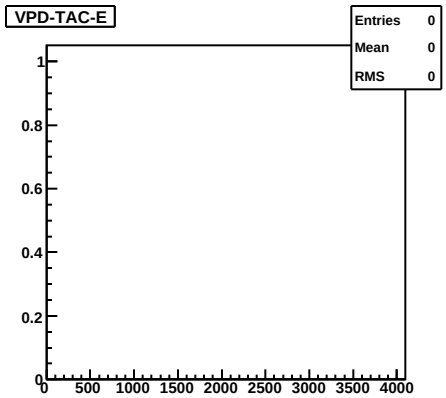

BBCsmall-TAC-W
Entries 0
Mean 0
RMS 0

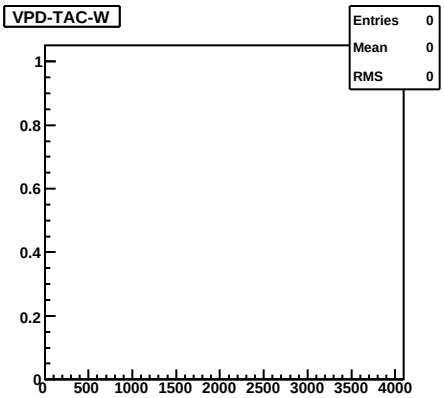

BBCsmall-TAC-DIFF = 4096 + BBCsmall-TAC-E - BBCsmall-TAC-W
Entries 0
Mean 0
RMS 0

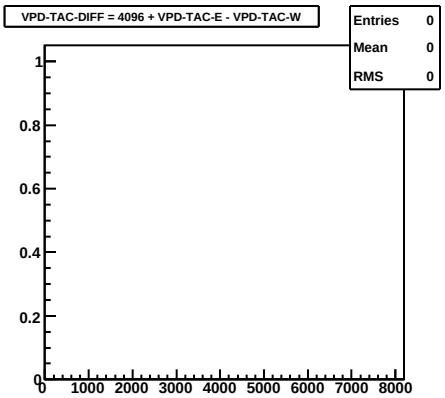

BBClarge-TAC-E
Entries 0
Mean 0
RMS 0

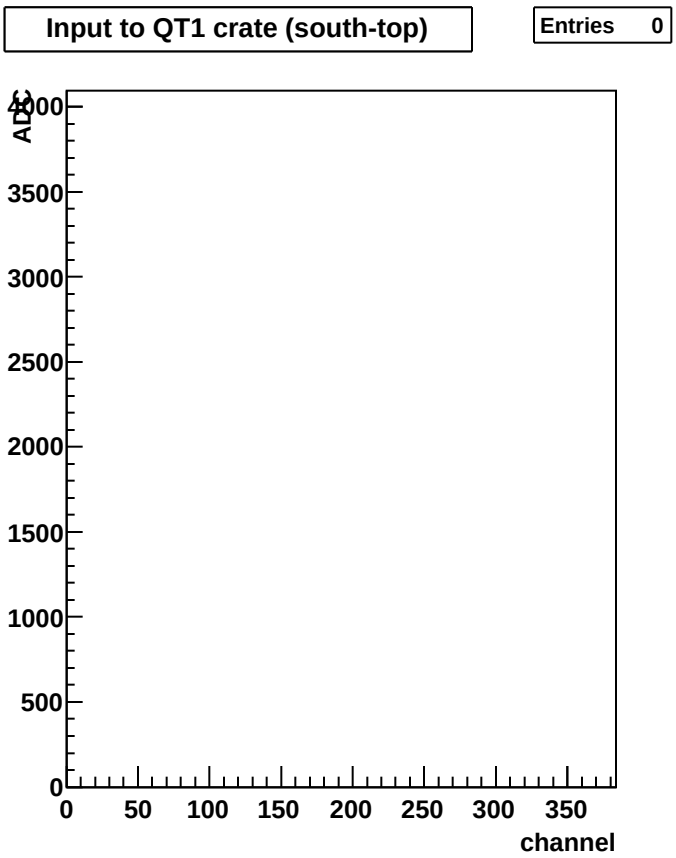

BBClarge-TAC-W
Entries 0
Mean 0
RMS 0

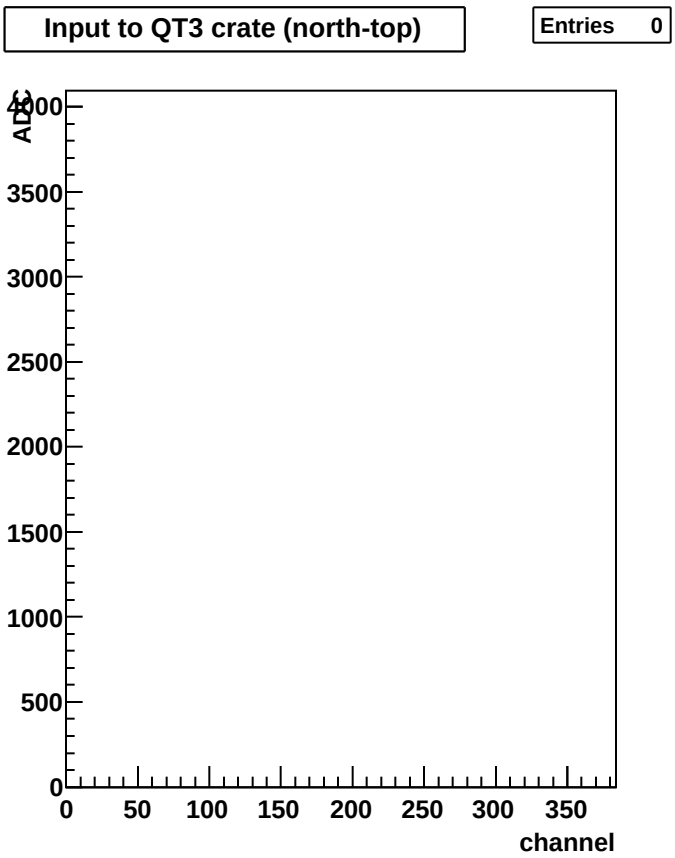

BBClarge-TAC-DIFF = 4096 + BBClarge-TAC-E - BBClarge-TAC-W
Entries 0
Mean 0
RMS 0

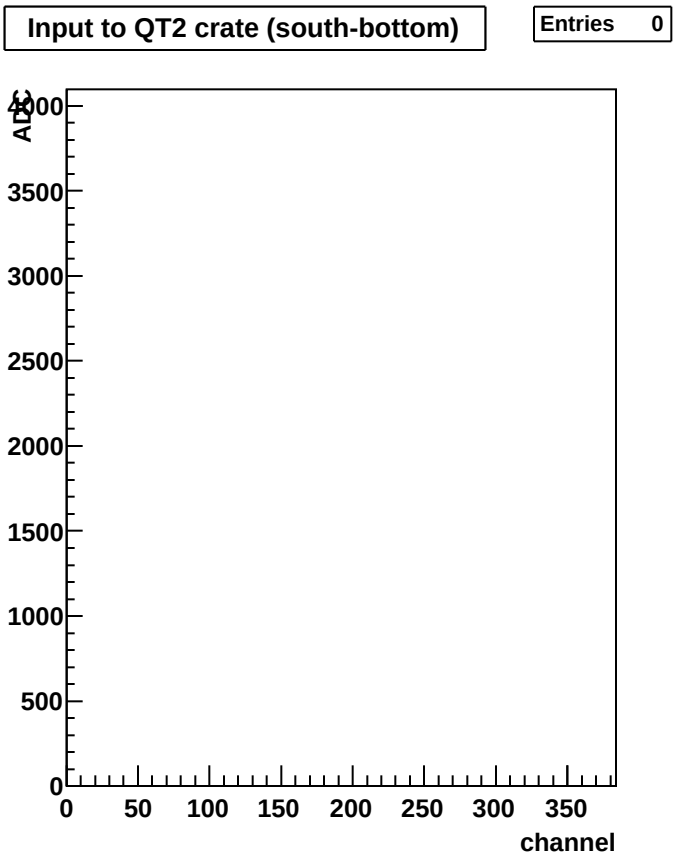

VPD-TAC-E
Entries 0
Mean 0
RMS 0

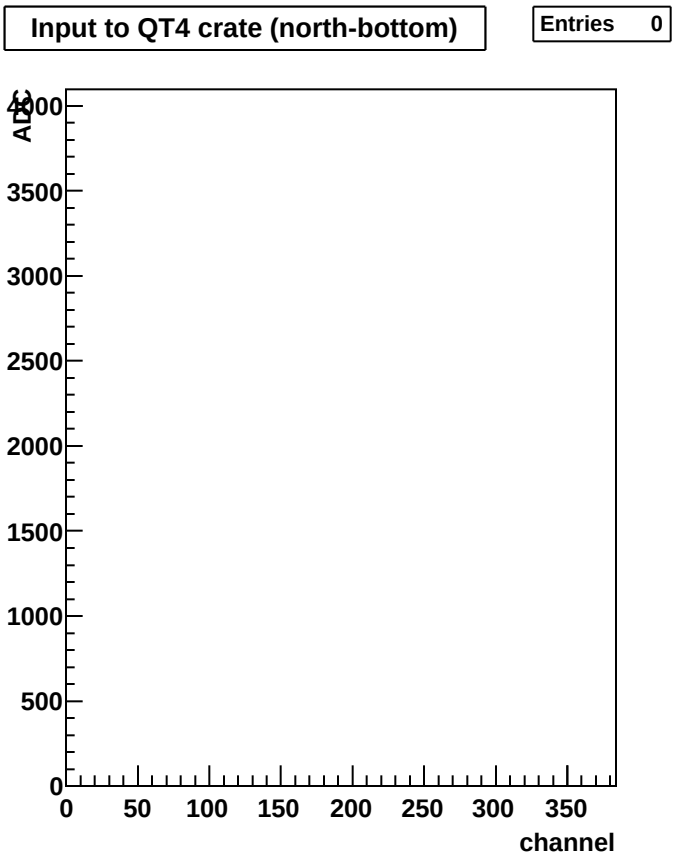

VPD-TAC-W
Entries 0
Mean 0
RMS 0

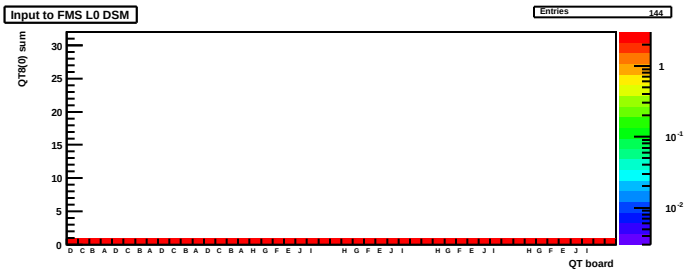

VPD-TAC-DIFF = 4096 + VPD-TAC-E - VPD-TAC-W
Entries 0
Mean 0
RMS 0

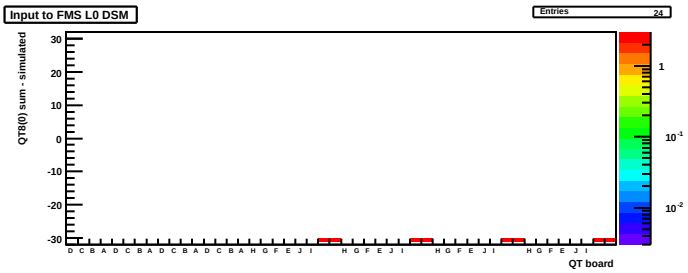

Input to QT1 crate (south-top)
Entries 0
ADC
4000
3500
3000
2500
2000
1500
1000
500
0
0 50 100 150 200 250 300 350
channel

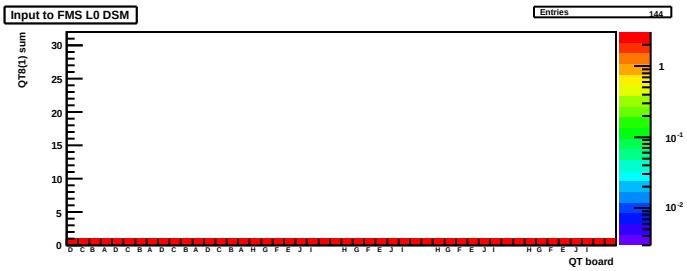

Input to QT3 crate (north-top)
Entries 0
ADC
4000
3500
3000
2500
2000
1500
1000
500
0
0 50 100 150 200 250 300 350
channel

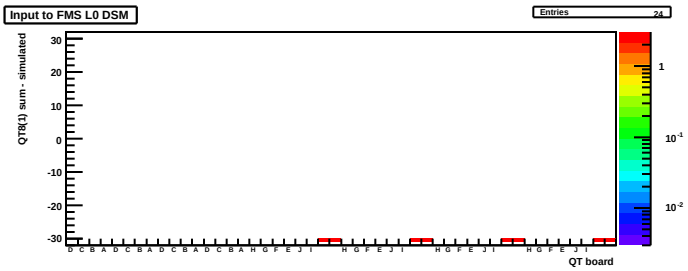

Input to QT2 crate (south-bottom)
Entries 0
ADC
4000
3500
3000
2500
2000
1500
1000
500
0
0 50 100 150 200 250 300 350
channel

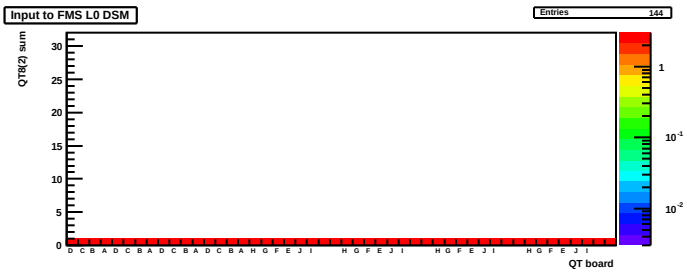

Input to QT4 crate (north-bottom)
Entries 0
ADC
4000
3500
3000
2500
2000
1500
1000
500
0
0 50 100 150 200 250 300 350
channel

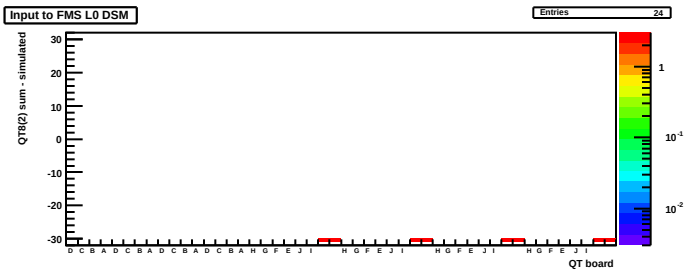

Input to FMS L0 DSM
Entries 144
QT8(0) sum
QT board

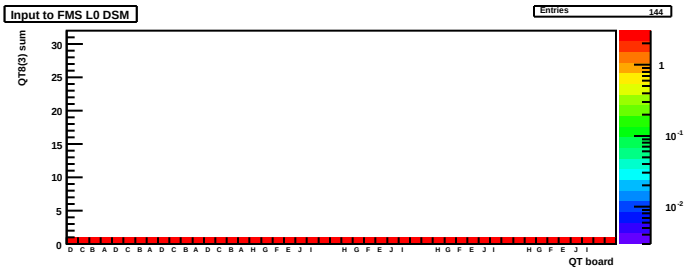

Input to FMS L0 DSM
Entries 24
QT8(0) sum - simulated
QT board

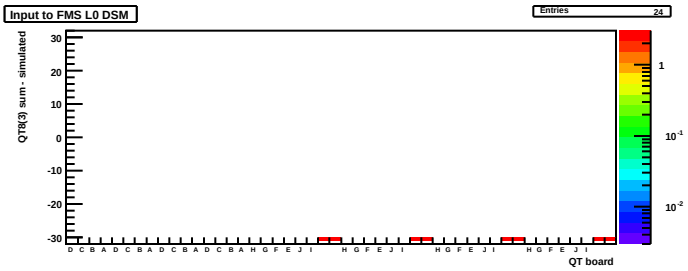

Input to FMS L0 DSM
Entries 144
QT8(1) sum
QT board

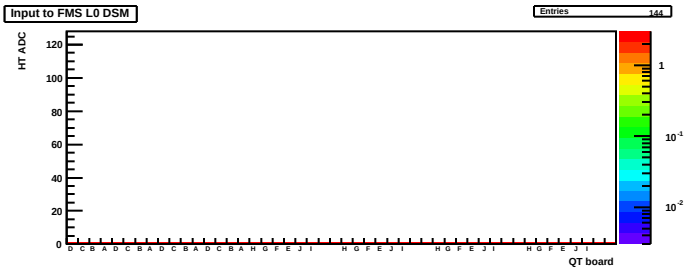

Input to FMS L0 DSM
Entries 24
QT8(1) sum - simulated
QT board

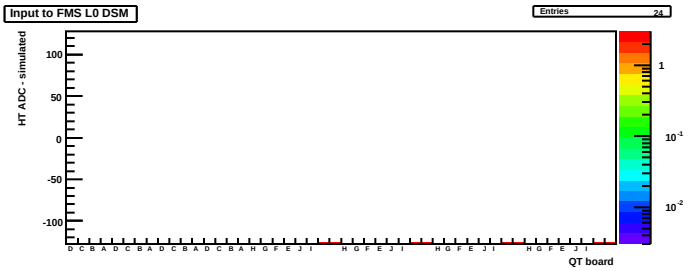

Input to FMS L0 DSM
Entries 144
QT8(2) sum
QT board

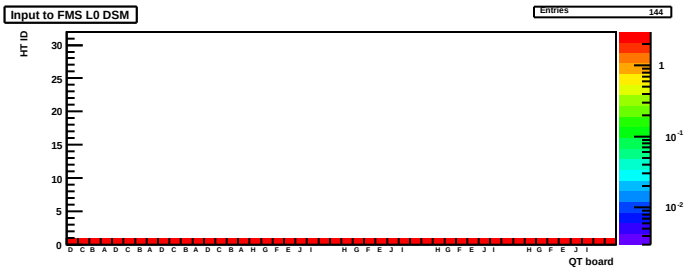

Input to FMS L0 DSM
Entries 24
QT8(2) sum - simulated
QT board

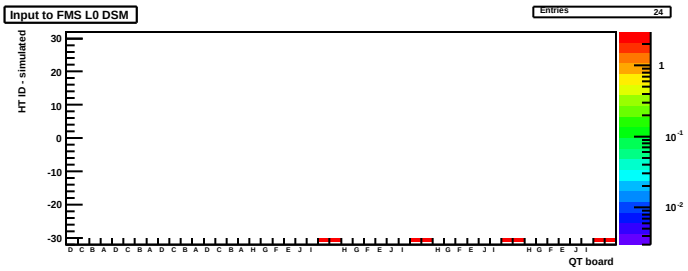

Input to FMS L0 DSM
Entries 144
QT8(3) sum
QT board

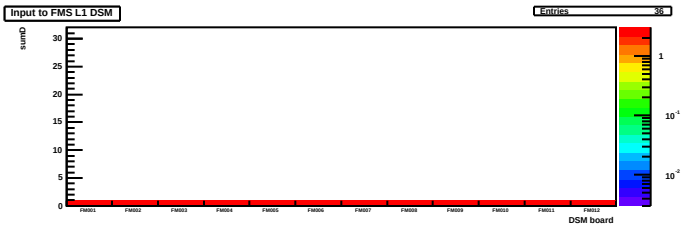

Input to FMS L0 DSM
Entries 24
QT8(3) sum - simulated
QT board

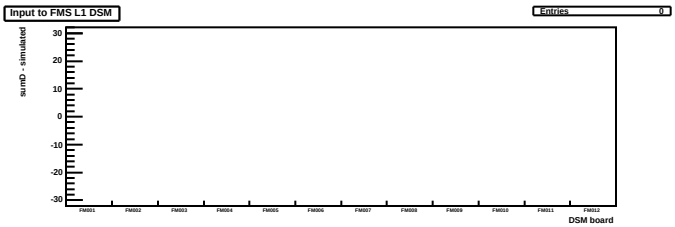

Input to FMS L0 DSM
Entries 144
HT ADC
QT board

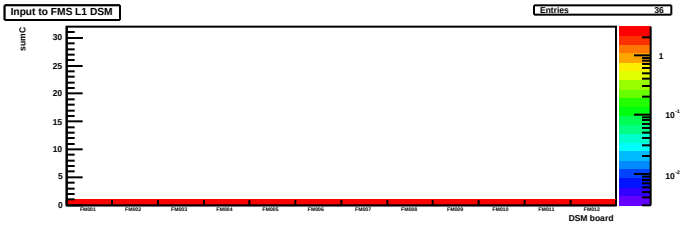

Input to FMS L0 DSM
Entries 24
HT ADC - simulated
QT board

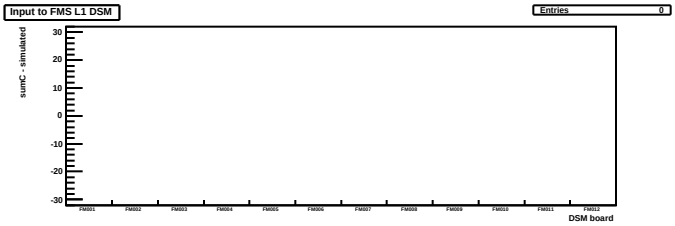

Input to FMS L0 DSM
Entries 144
HT ID
QT board

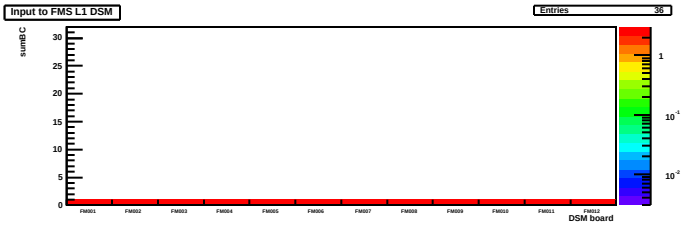

Input to FMS L0 DSM
Entries 24
HT ID - simulated
QT board

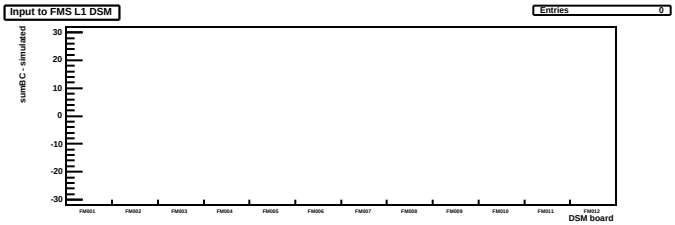

Input to FMS L1 DSM
Entries 36
sumD
DSM board

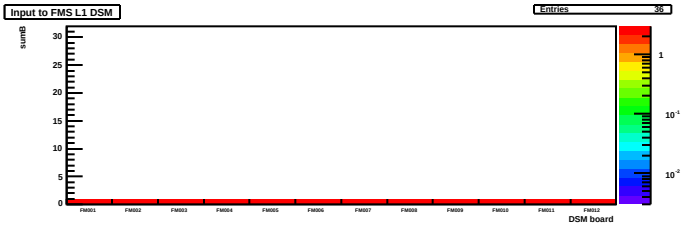

Input to FMS L1 DSM
Entries 0
sumD - simulated
DSM board

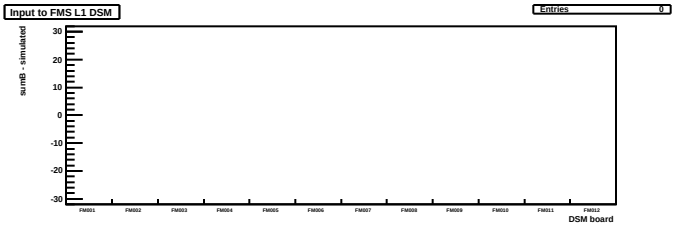

Input to FMS L1 DSM
Entries 36
sumC
DSM board

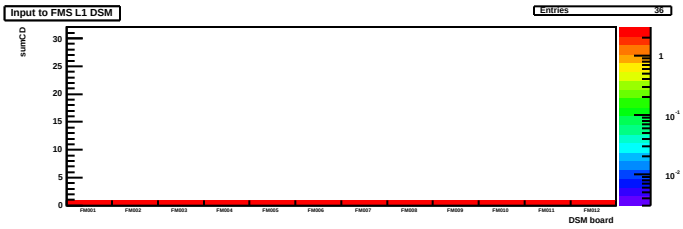

Input to FMS L1 DSM
Entries 0
sumC - simulated
DSM board

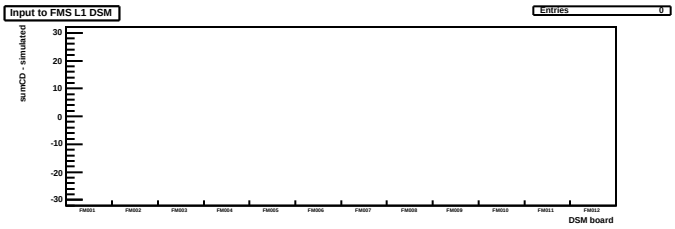

Input to FMS L1 DSM
Entries 36
sumBC
DSM board

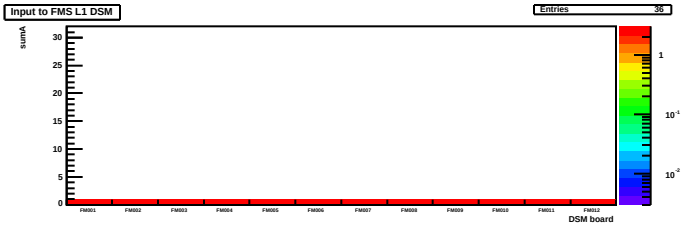

Input to FMS L1 DSM
Entries 0
sumBC - simulated
DSM board

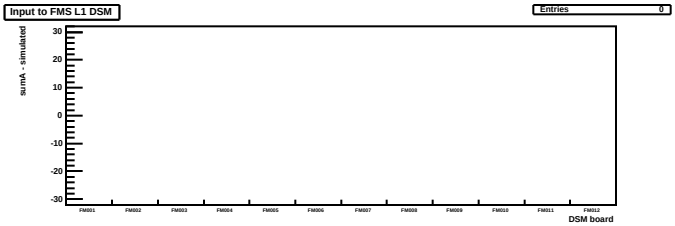

Input to FMS L1 DSM
Entries 36
sumB
DSM board

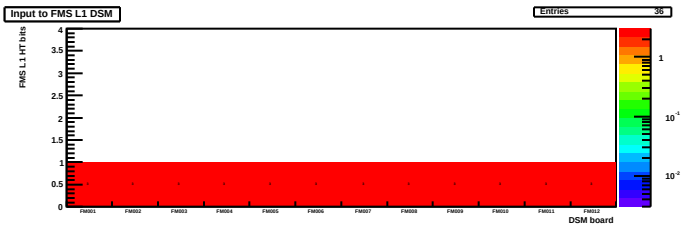

Input to FMS L1 DSM
Entries 0
sumB - simulated
DSM board

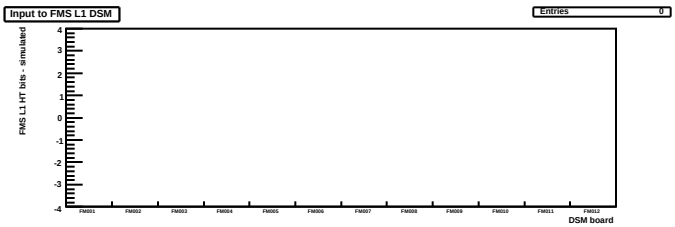

Input to FMS L1 DSM
Entries 36
sumCD
DSM board

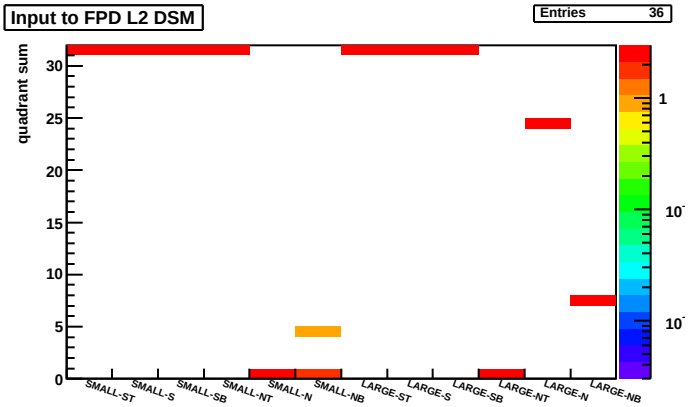

Input to FMS L1 DSM
Entries 0
sumCD - simulated
DSM board

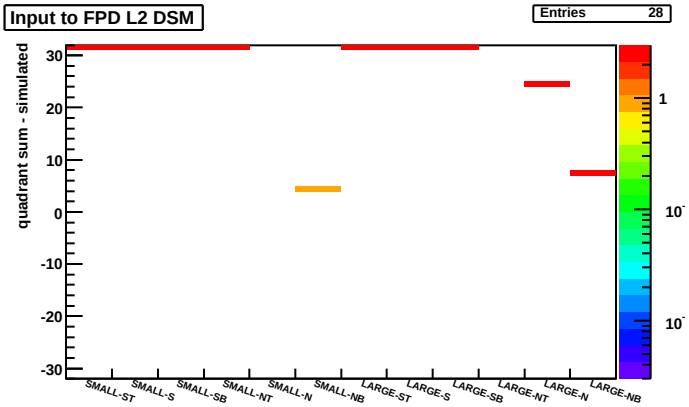

Input to FMS L1 DSM
Entries 36
sumA
DSM board

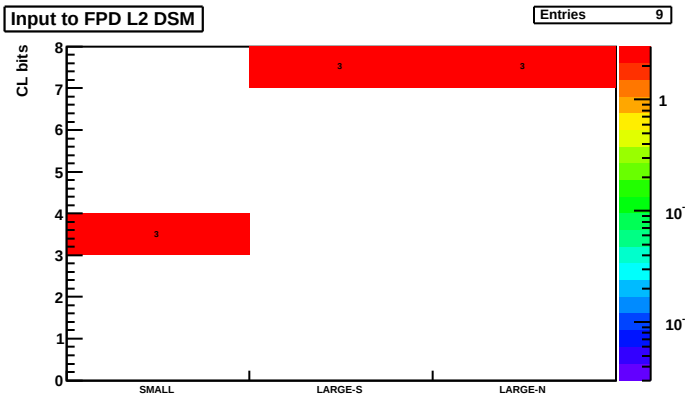

Input to FMS L1 DSM
Entries 0
sumA - simulated
DSM board

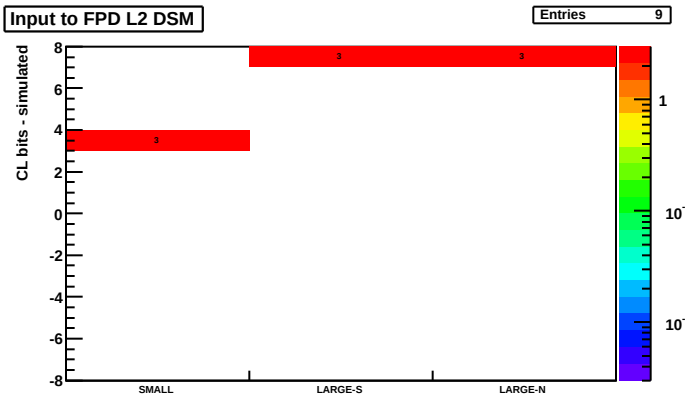

Input to FMS L1 DSM
Entries 36
FMS L1 HT bits
DSM board

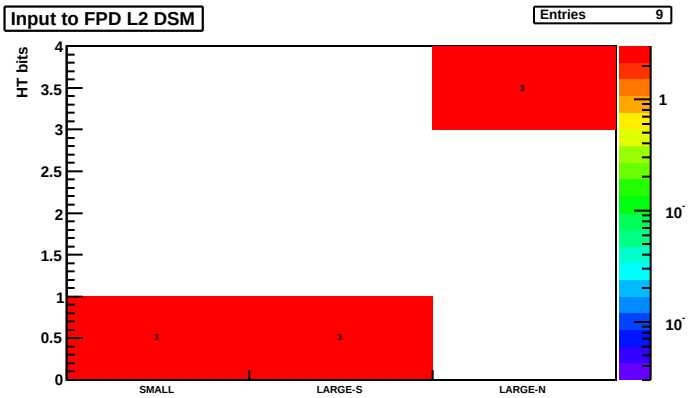

Input to FMS L1 DSM
Entries 0
FMS L1 HT bits - simulated
DSM board

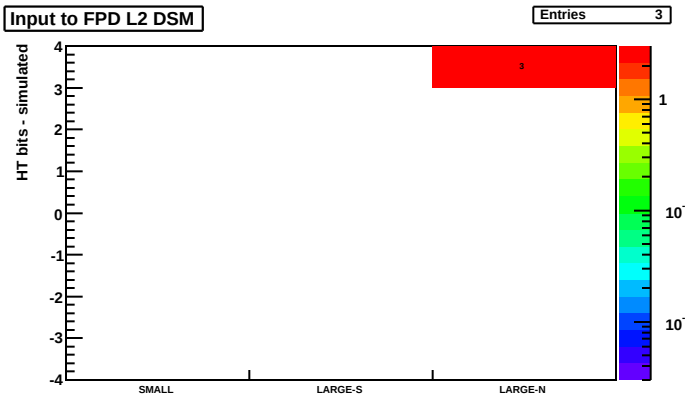

Input to FPD L2 DSM
Entries 36
quadrant sum
SMALL-ST
SMALL-S
SMALL-SB
SMALL-NT
SMALL-N
SMALL-NB
LARGE-ST
LARGE-S
LARGE-SB
LARGE-NT
LARGE-N
LARGE-NB

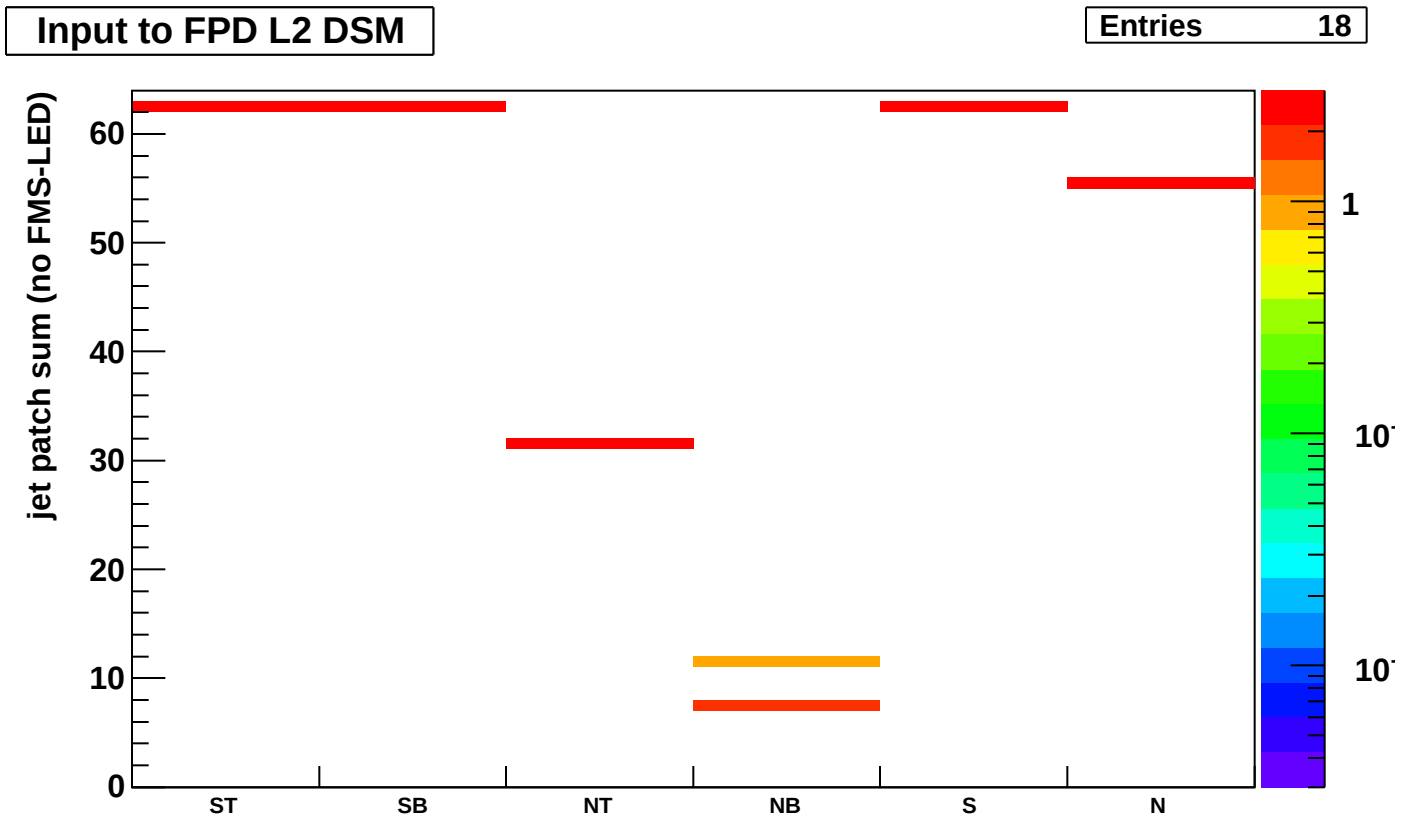

Input to FPD L2 DSM
Entries 28
quadrant sum - simulated
SMALL-ST
SMALL-S
SMALL-SB
SMALL-NT
SMALL-N
SMALL-NB
LARGE-ST
LARGE-S
LARGE-SB
LARGE-NT
LARGE-N
LARGE-NB

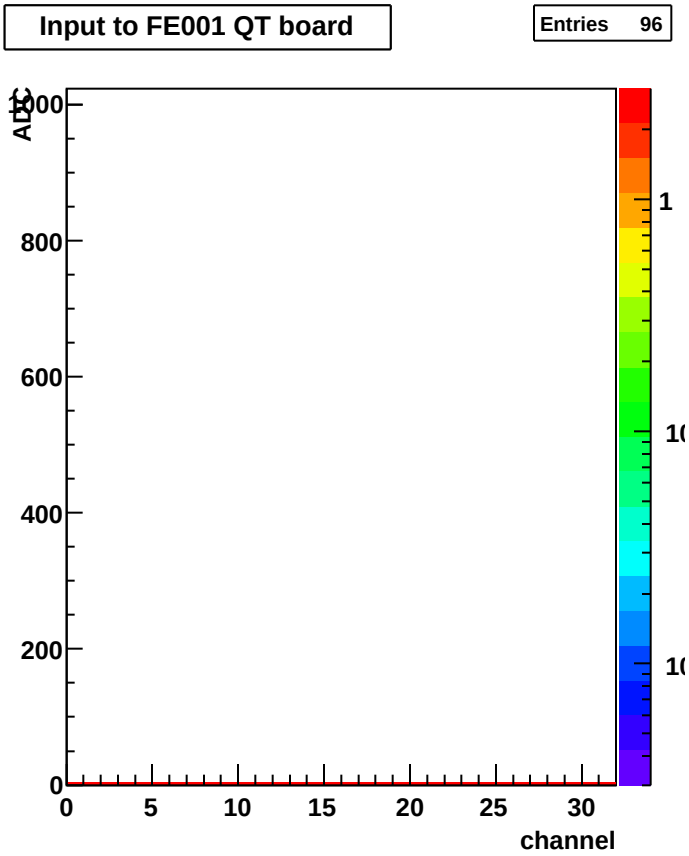

Input to FPD L2 DSM
Entries 9
CL bits
SMALL
LARGE-S
LARGE-N

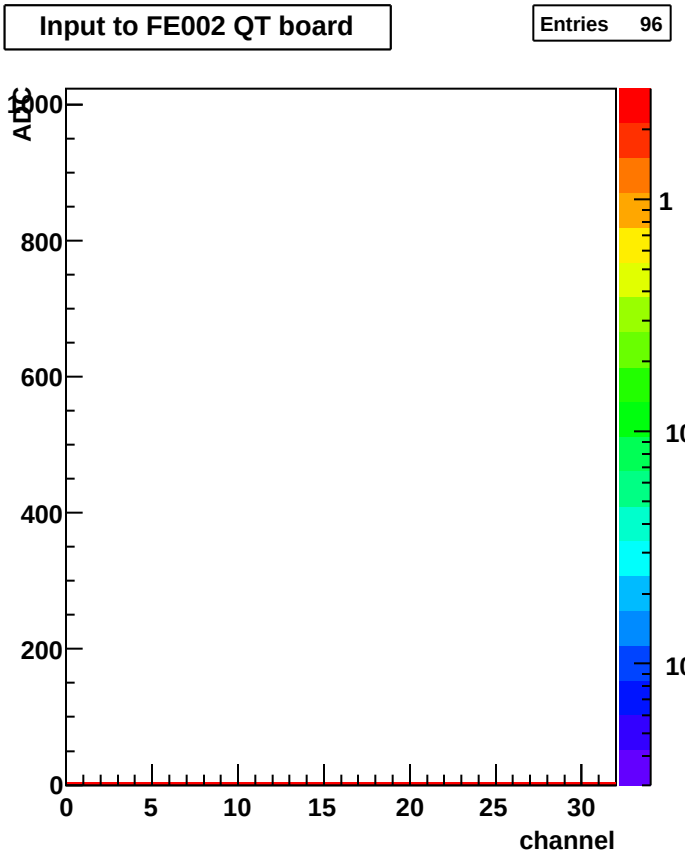

Input to FPD L2 DSM
Entries 9
CL bits - simulated
SMALL
LARGE-S
LARGE-N

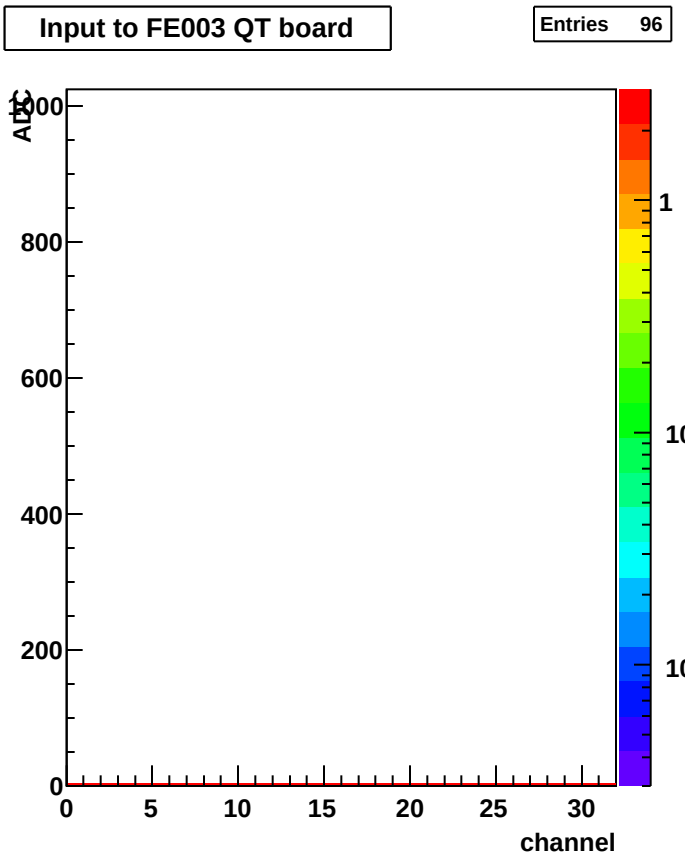

Input to FPD L2 DSM
Entries 9
HT bits
SMALL
LARGE-S
LARGE-N

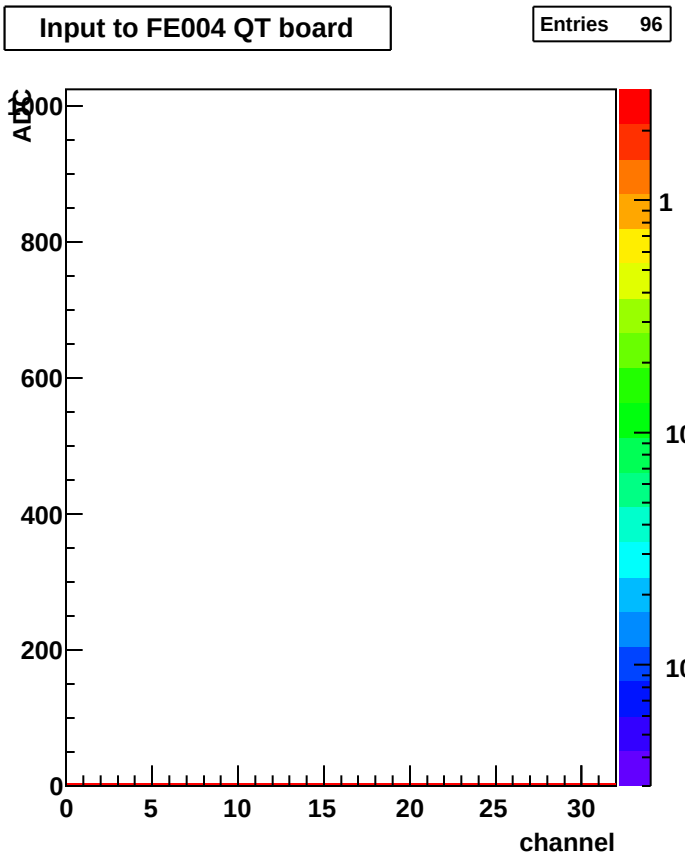

Input to FPD L2 DSM
Entries 3
HT bits - simulated
SMALL
LARGE-S
LARGE-N

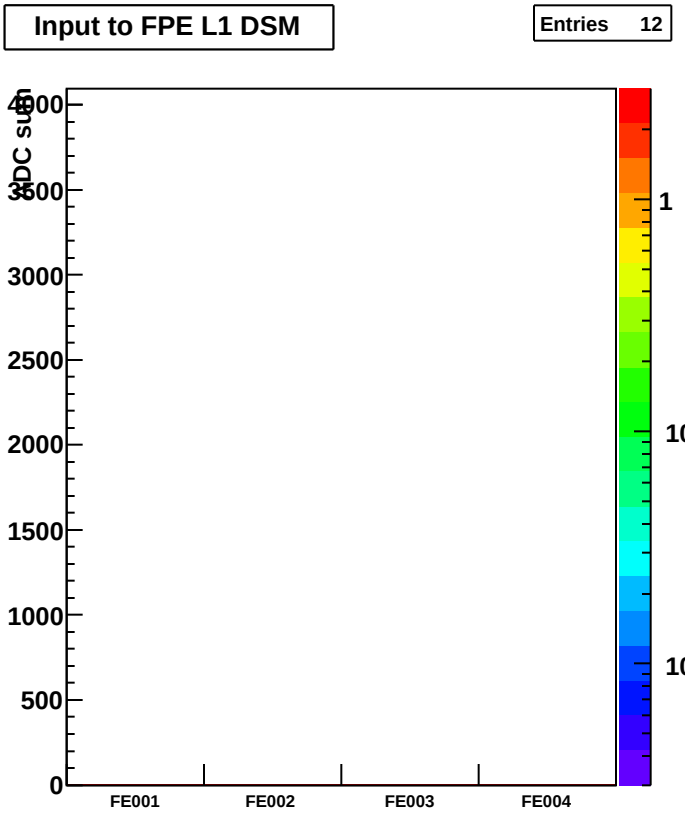

Input to FPD L2 DSM
Entries 18
jet patch sum (no FMS-LED)
0
10
20
30
40
50
60
ST
SB
NT
NB
S
N
1

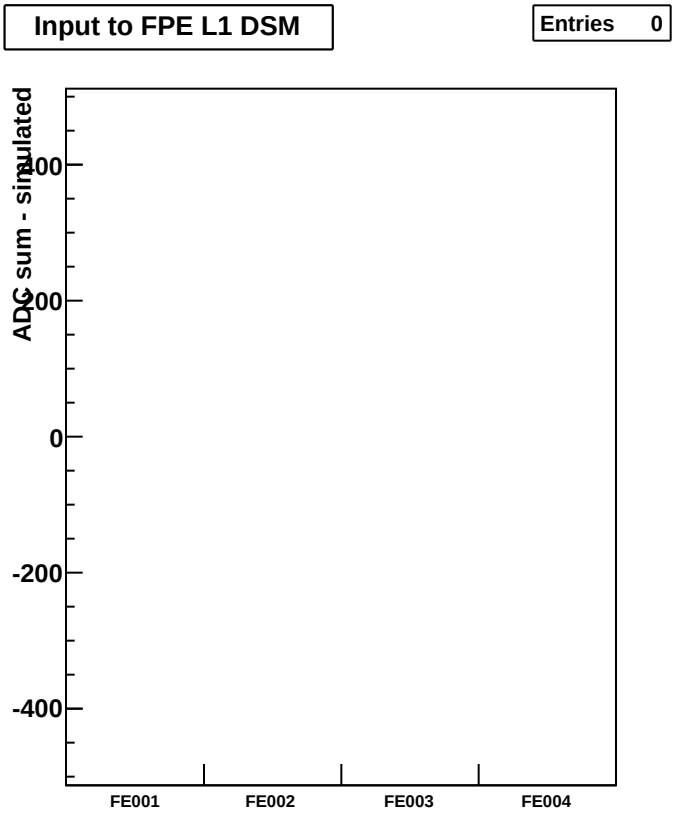

Input to FE001 QT board
Entries 96
ADC
channel

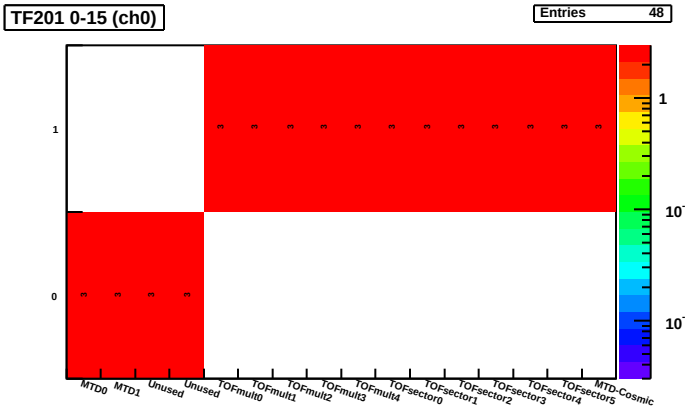

Input to FE002 QT board
Entries 96
ADC
channel

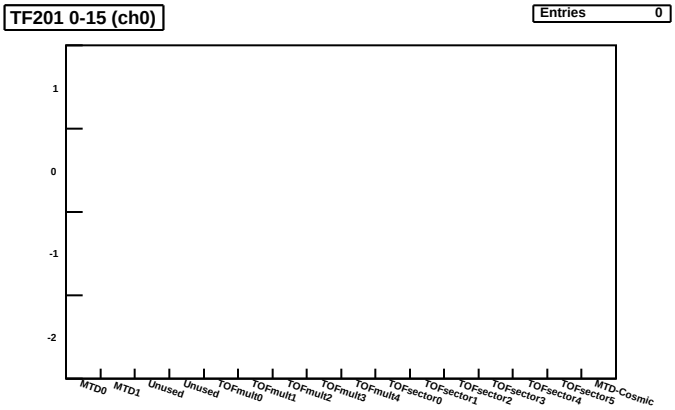

Input to FE003 QT board
Entries 96
ADC
channel

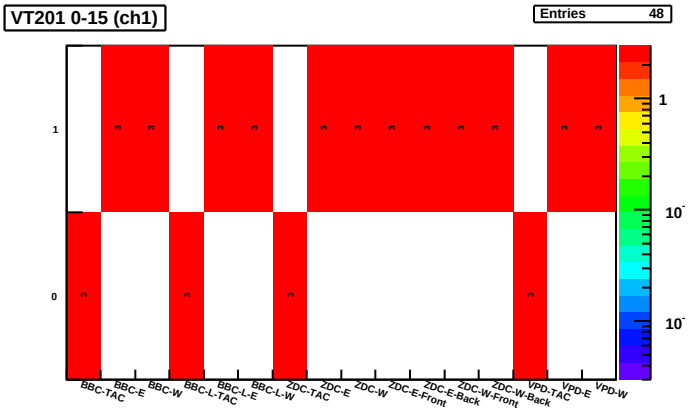

Input to FE004 QT board
Entries 96
ADC
channel

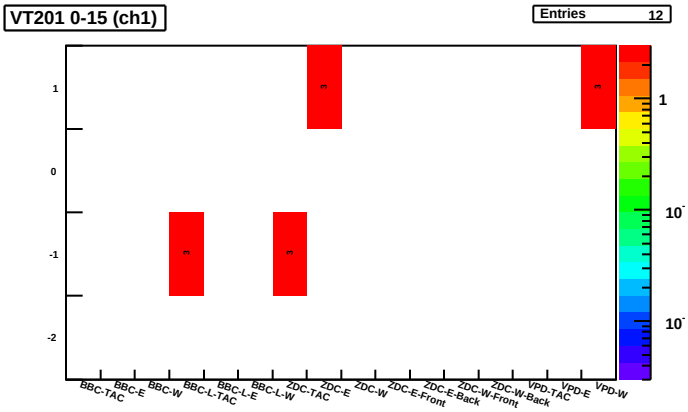

Input to FPE L1 DSM
Entries 12
ADC sum
4000
3500
3000
2500
2000
1500
1000
500
0
FE001
FE002
FE003
FE004
1
10
10

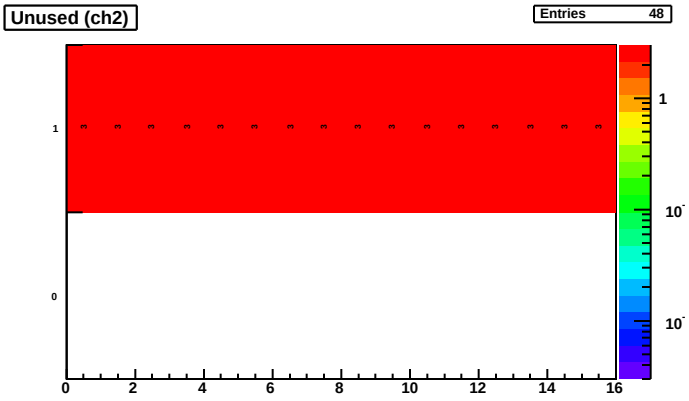

Input to FPE L1 DSM
Entries 0
ADC sum - simulated
100
200
0
-200
-400
FE001
FE002
FE003
FE004

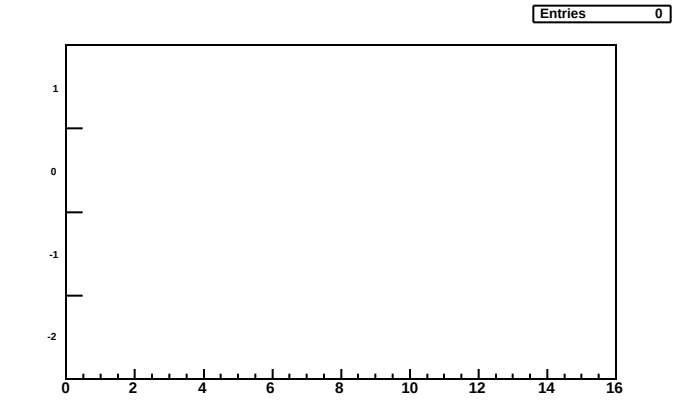

TF201 0-15 (ch0)
Entries 48
MTD0 MTD1 Unused Unused TOFmult0 TOFmult1 TOFmult2 TOFmult3 TOFmult4 TOFsector0 TOFsector1 TOFsector2 TOFsector3 TOFsector4 TOFsector5 MTD-Cosmic

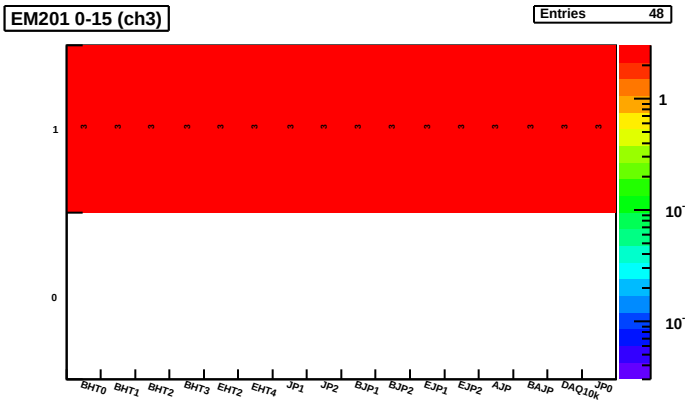

TF201 0-15 (ch0)
Entries 0
MTD0 MTD1 Unused Unused TOFmult0 TOFmult1 TOFmult2 TOFmult3 TOFmult4 TOFsector0 TOFsector1 TOFsector2 TOFsector3 TOFsector4 TOFsector5 MTD-Cosmic

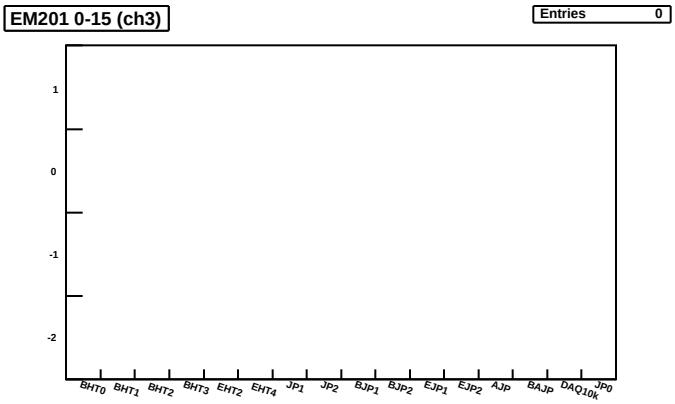

VT201 0-15 (ch1)
Entries 48
BBC-TAC BBC-E BBC-W BBC-L-TAC BBC-L-E BBC-L-W ZDC-TAC ZDC-E ZDC-W ZDC-E-Front ZDC-E-Back ZDC-W-Front ZDC-W-Back VPD-TAC VPD-E VPD-W


VT201 0-15 (ch1)
Entries 12
BBC-TAC BBC-E BBC-W BBC-L-TAC BBC-L-E BBC-L-W ZDC-TAC ZDC-E ZDC-W ZDC-E-Front ZDC-E-Back ZDC-W-Front ZDC-W-Back VPD-TAC VPD-E VPD-W

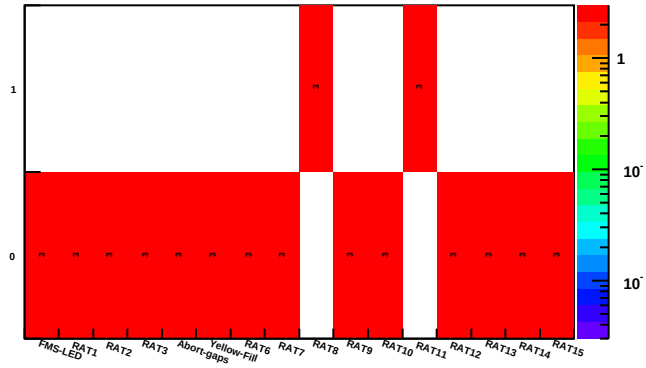

Unused (ch2)
Entries 48

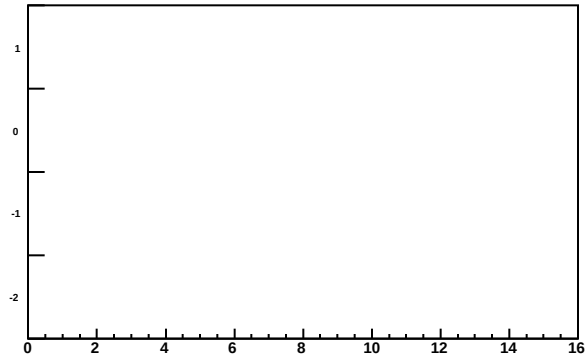

Entries 0


EM201 0-15 (ch3)
Entries 48
BHT0 BHT1 BHT2 BHT3 EHT2 EHT4 JP1 JP2 BJP1 BJP2 EJP1 EJP2 AJP BAJP DAQ10k JP0

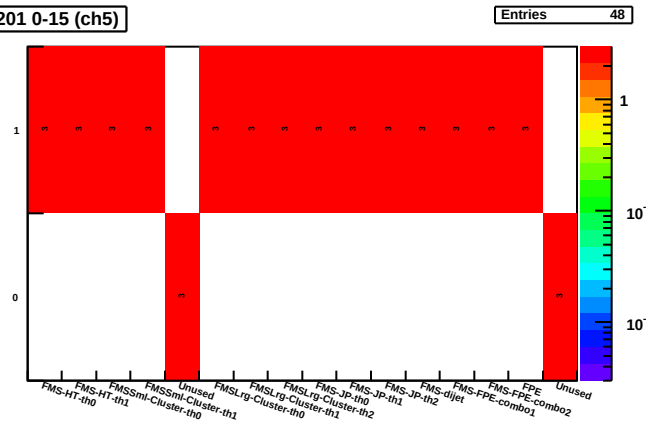

EM201 0-15 (ch3)
Entries 0
BHT0 BHT1 BHT2 BHT3 EHT2 EHT4 JP1 JP2 BJP1 BJP2 EJP1 EJP2 AJP BAJP DAQ10k JP0

RAT board (ch4)

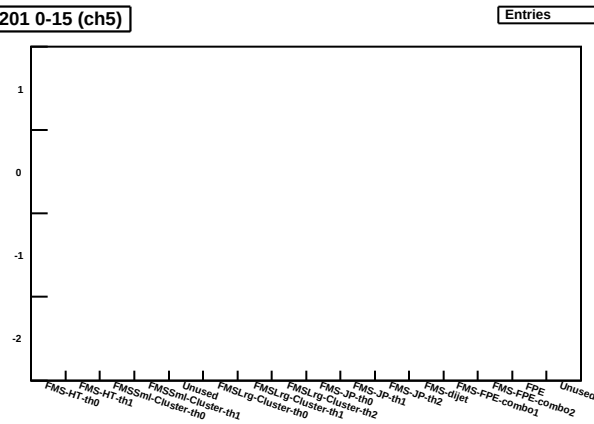




FP201 0-15 (ch5)



FP201 0-15 (ch5)



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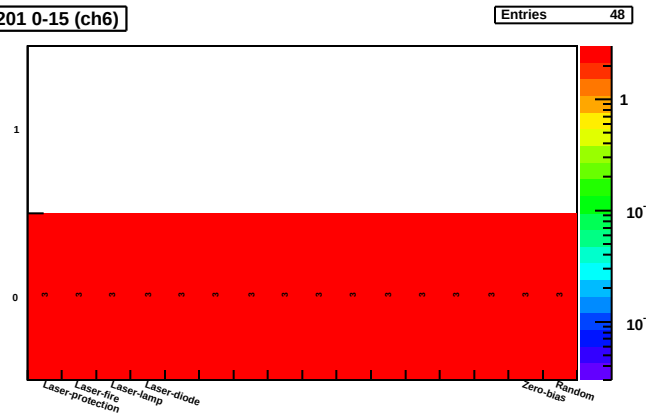

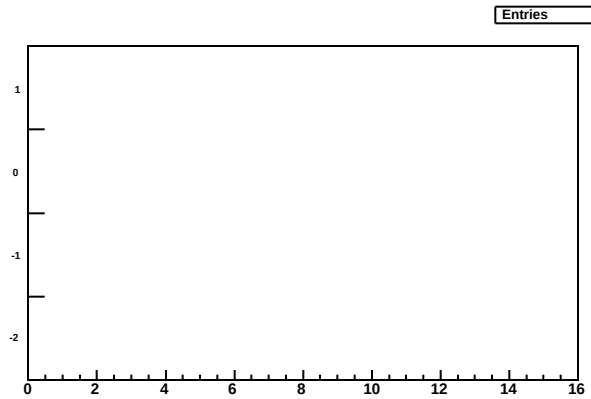
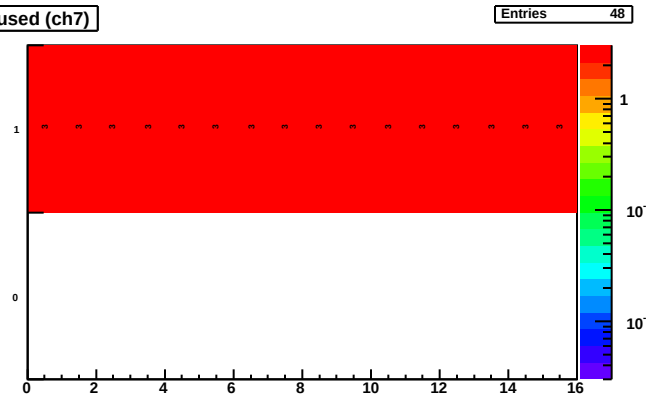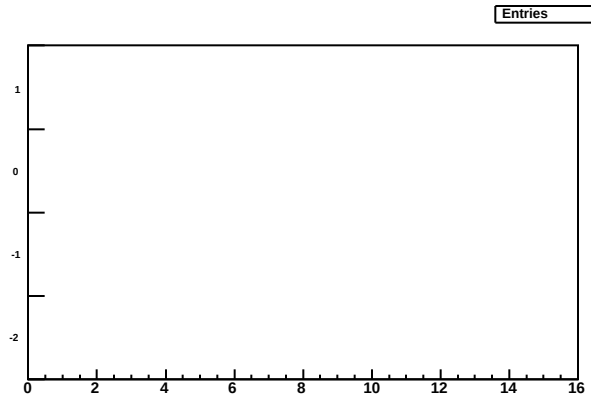
Unused (ch7)