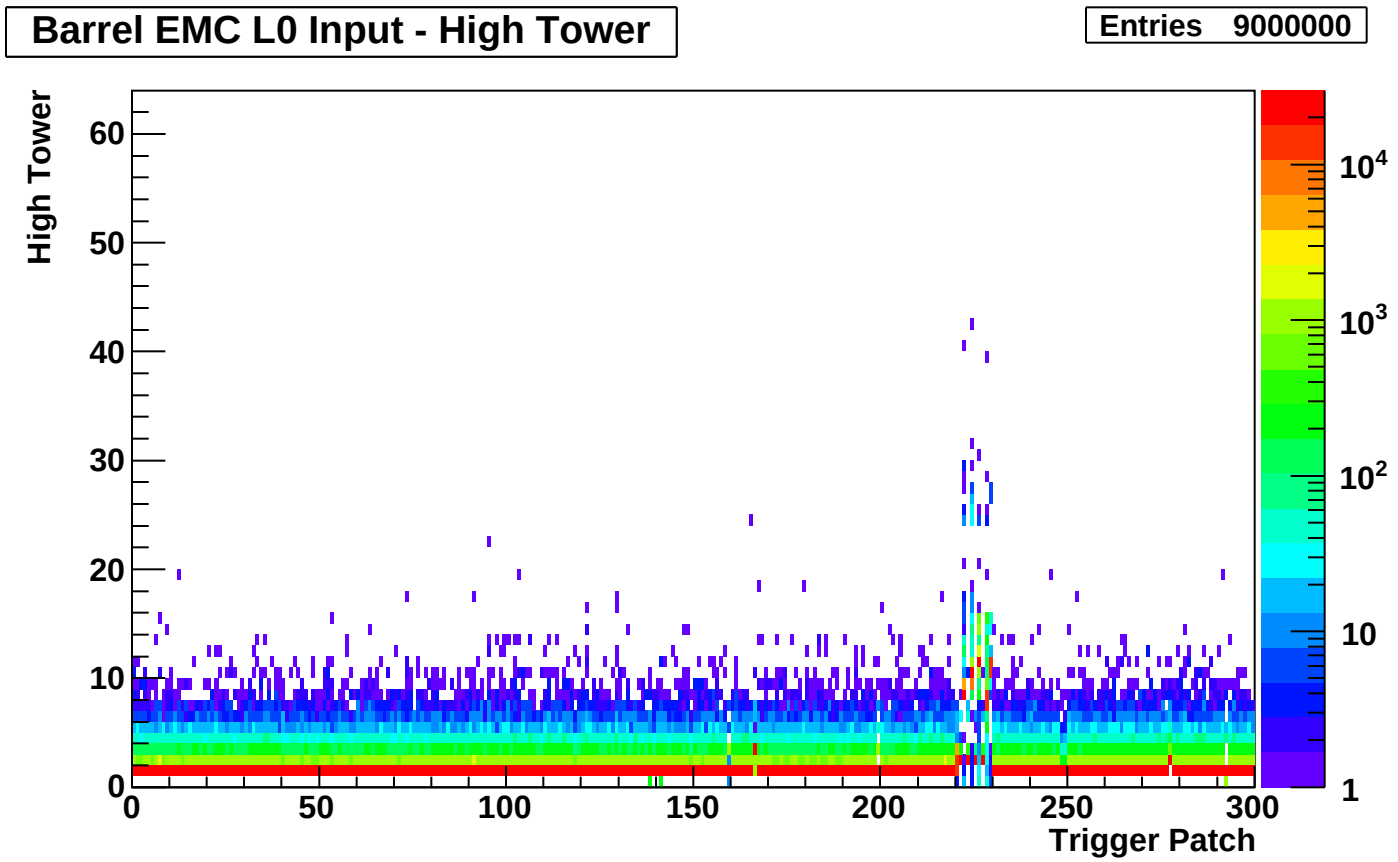
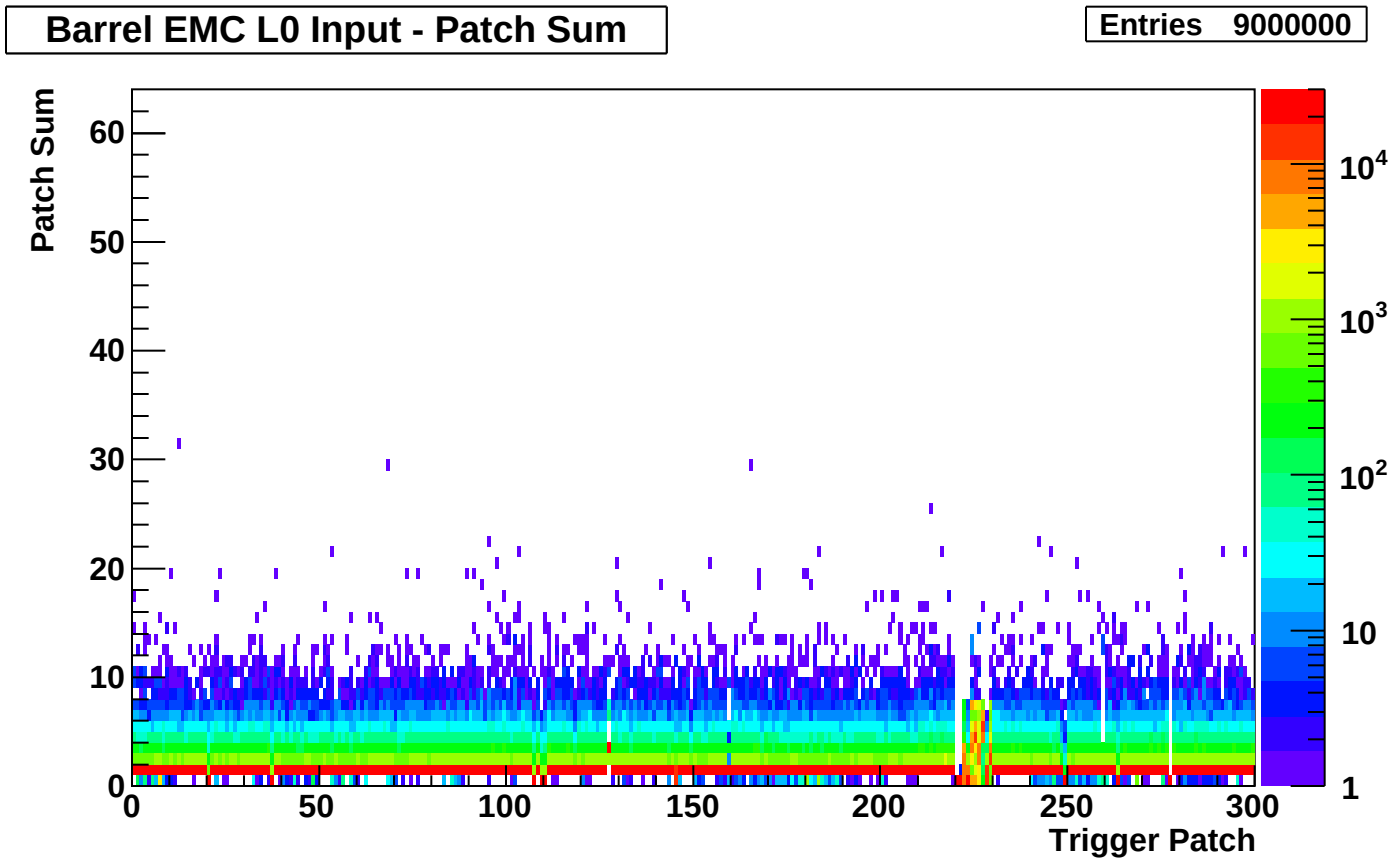
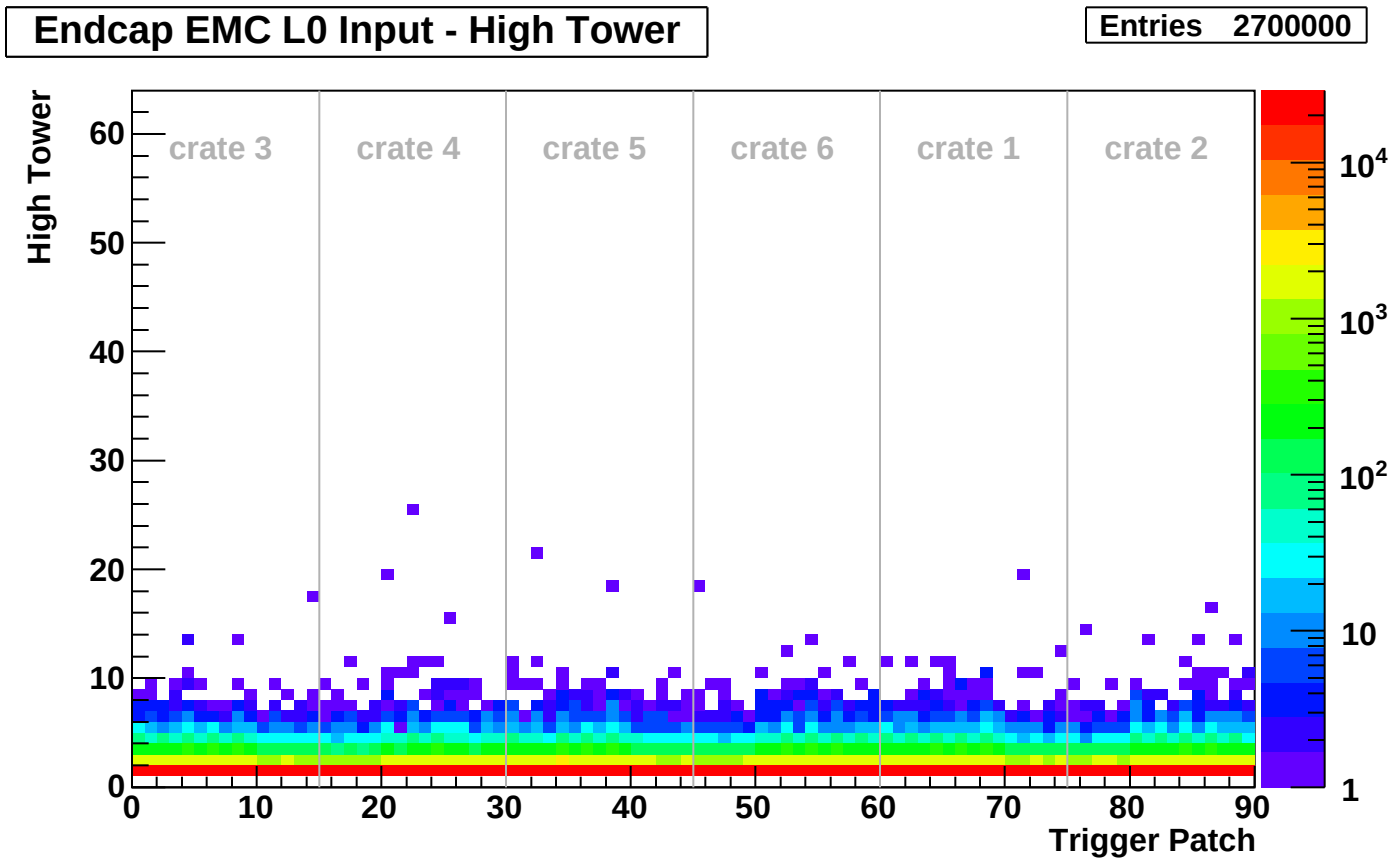
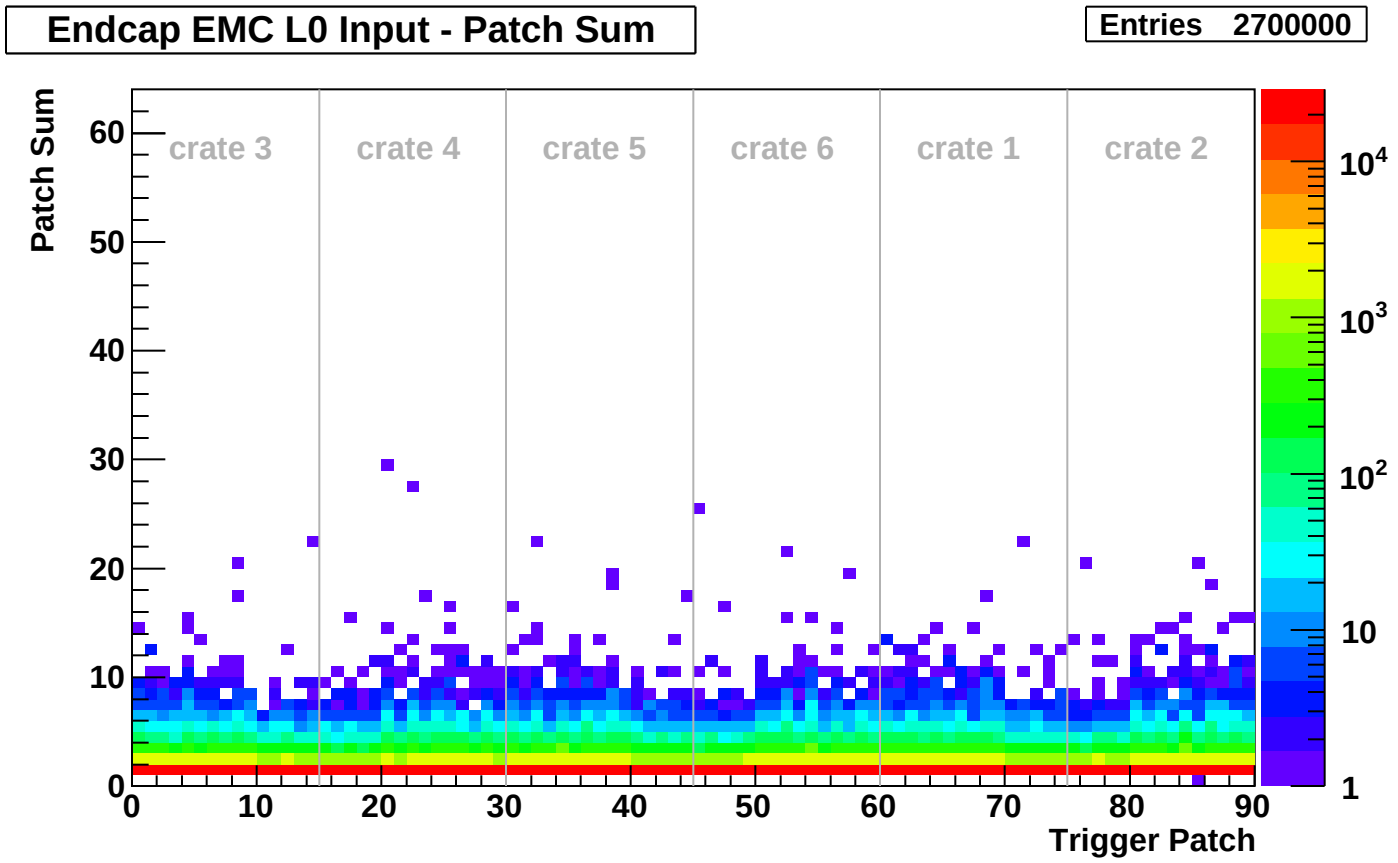
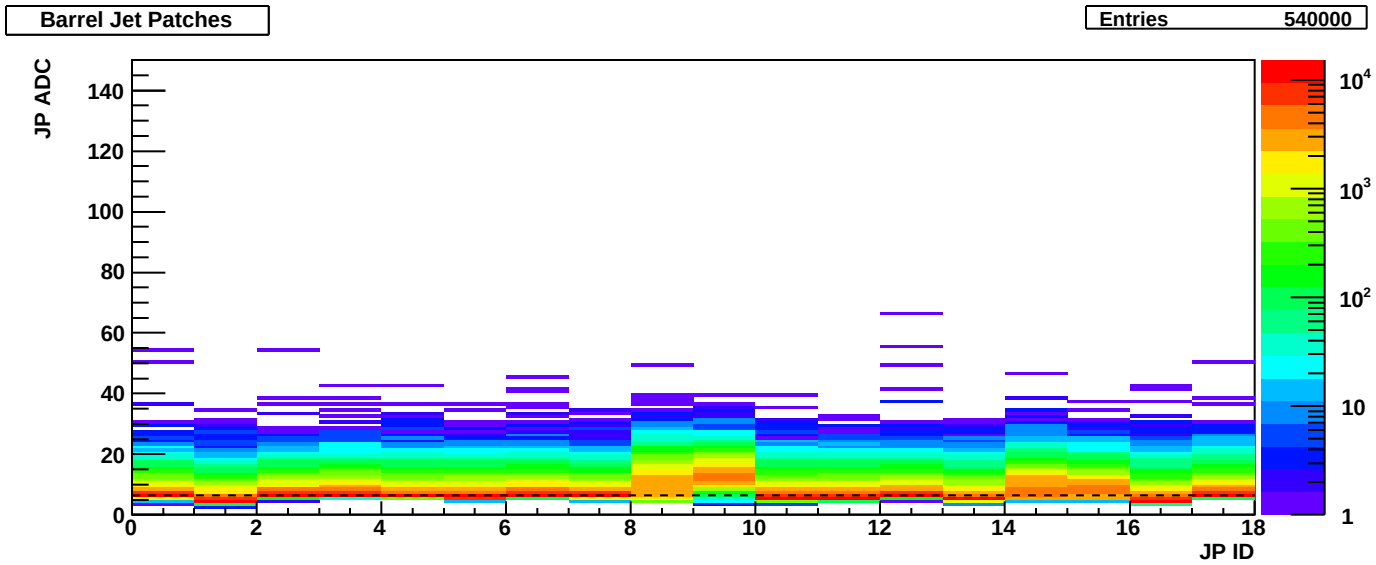
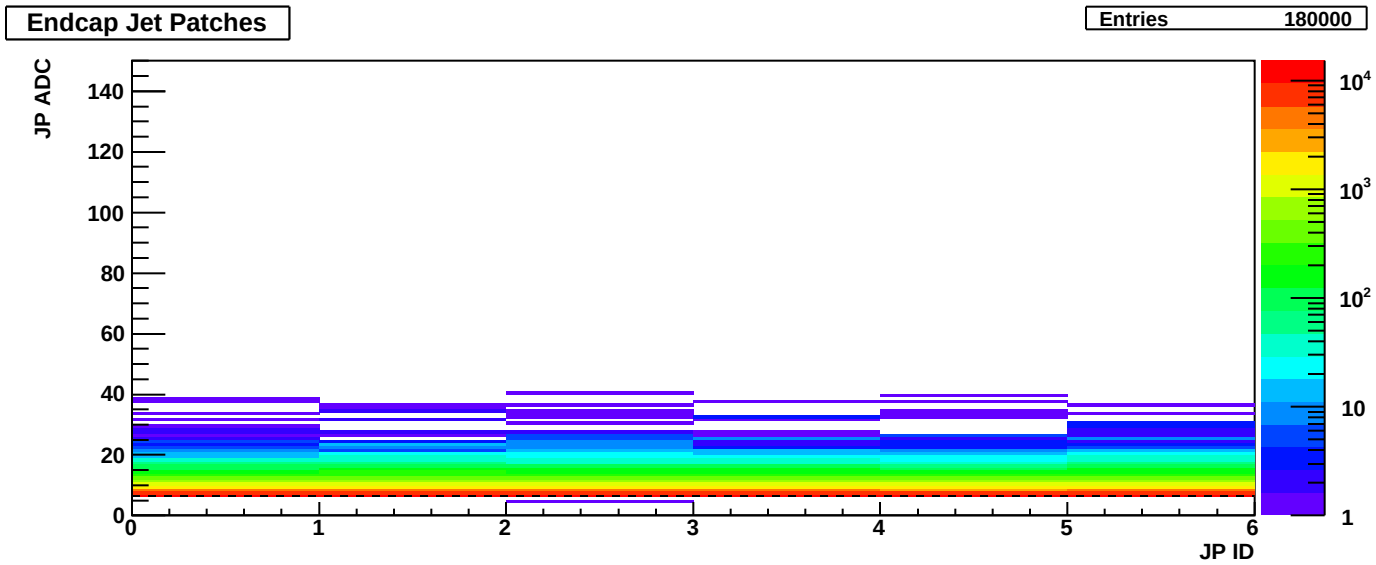

Barrel EMC L0 Input - High Tower
Entries 9000000
High Tower
Trigger Patch
0
10
20
30
40
50
60
0
50
100
150
200
250
300
1
10
10^2
10^3
10^4

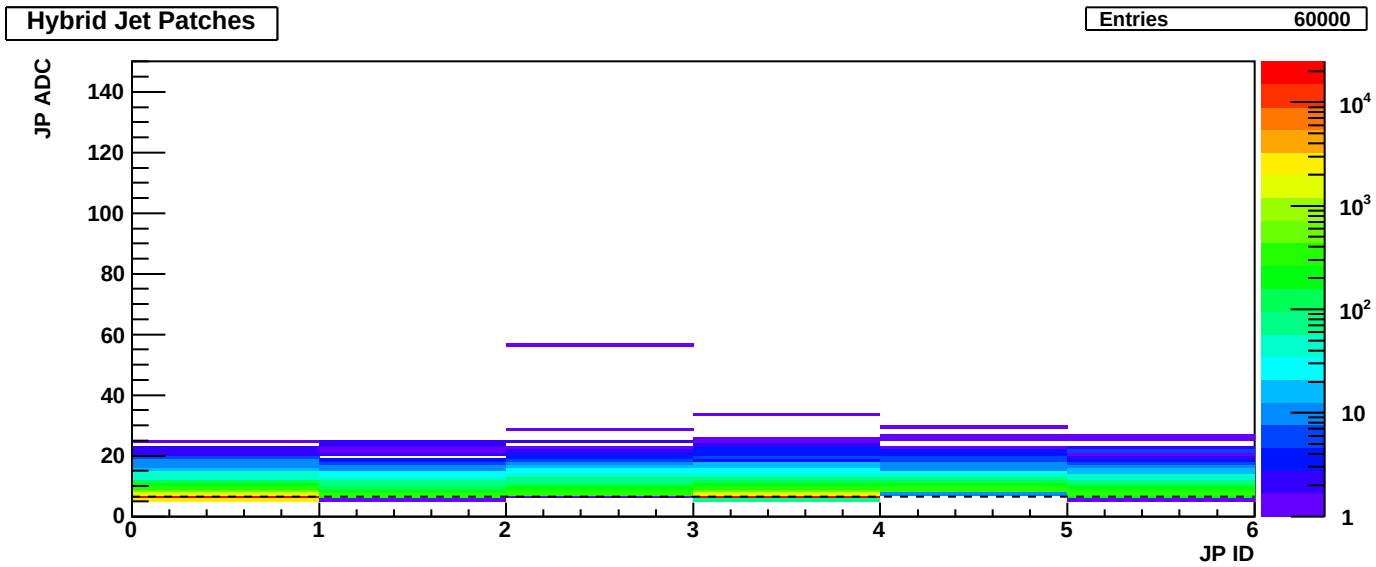

Barrel EMC L0 Input - Patch Sum
Entries 9000000
Patch Sum
Trigger Patch
0
10
20
30
40
50
60
0
50
100
150
200
250
300
1
10
10^2
10^3
10^4

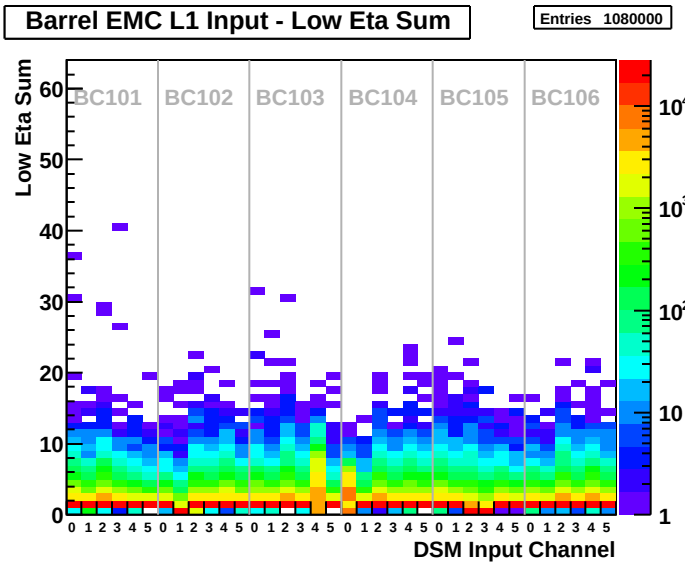

Endcap EMC L0 Input - High Tower
Entries 2700000
High Tower
crate 3
crate 4
crate 5
crate 6
crate 1
crate 2
Trigger Patch

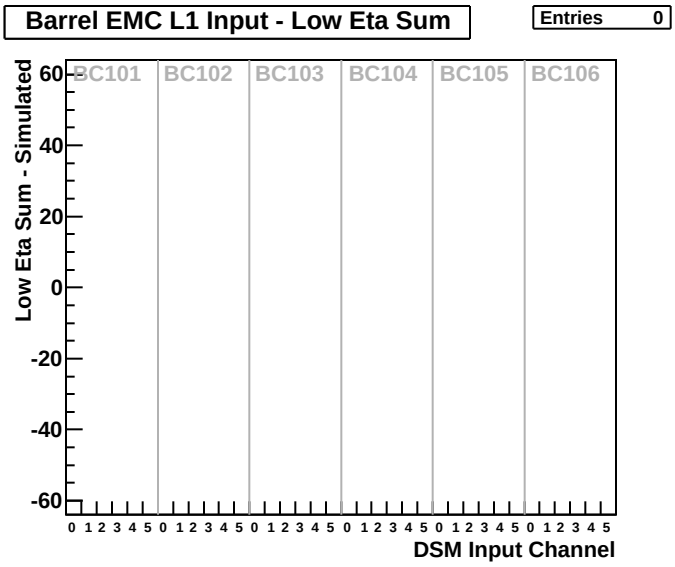

Endcap EMC L0 Input - Patch Sum
Entries 2700000
Patch Sum
crate 3
crate 4
crate 5
crate 6
crate 1
crate 2
Trigger Patch

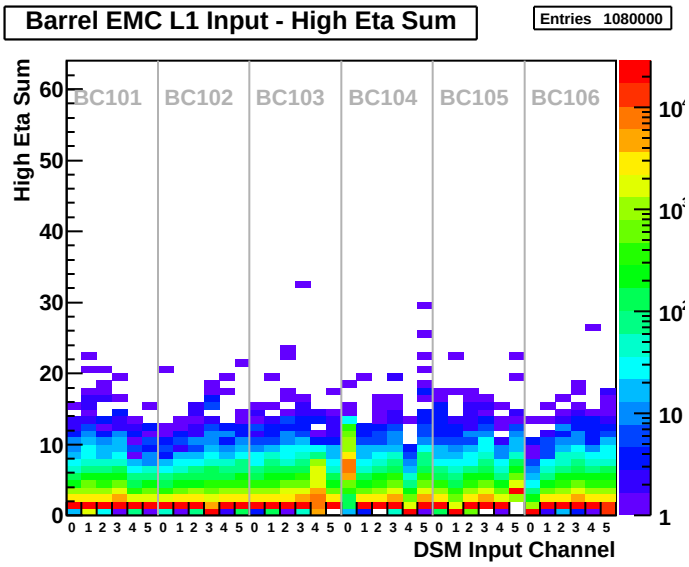

Barrel Jet Patches
Entries 540000
JP ADC
JP ID

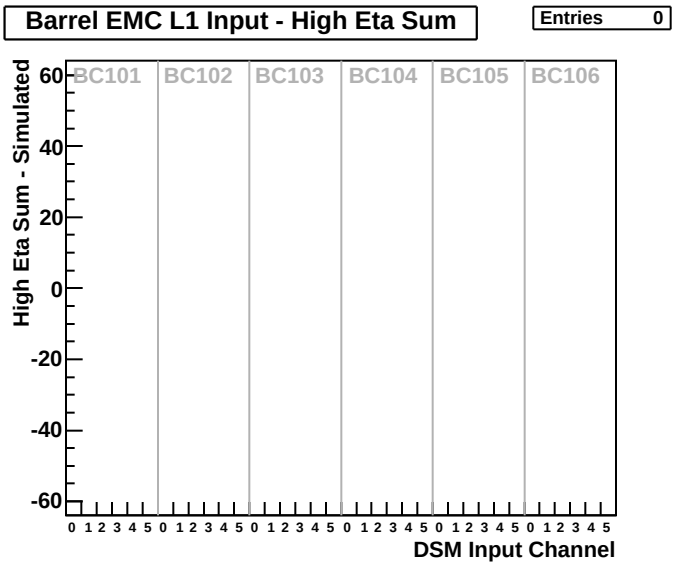

Endcap Jet Patches
Entries 180000
JP ADC
JP ID

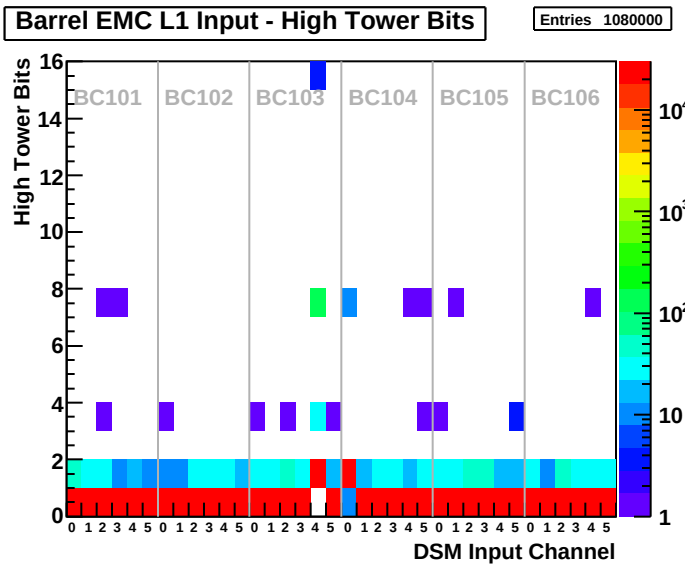

Hybrid Jet Patches
Entries 60000
JP ADC
JP ID

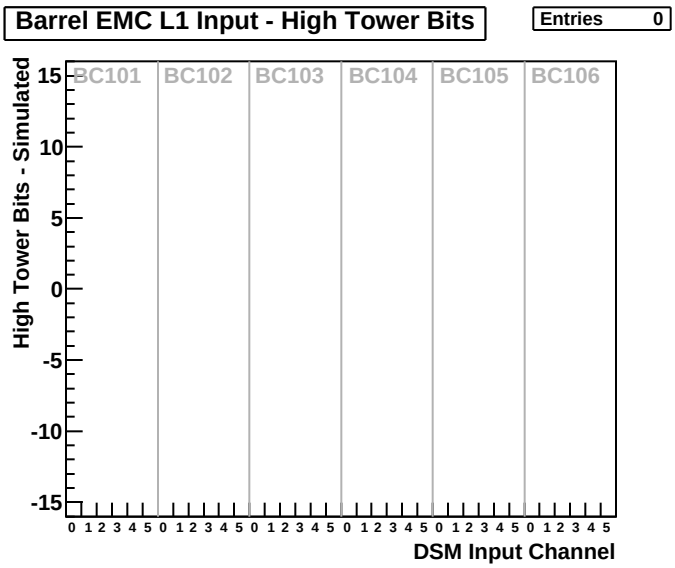

Barrel EMC L1 Input - Low Eta Sum
Entries 1080000
Low Eta Sum
BC101
BC102
BC103
BC104
BC105
BC106
DSM Input Channel

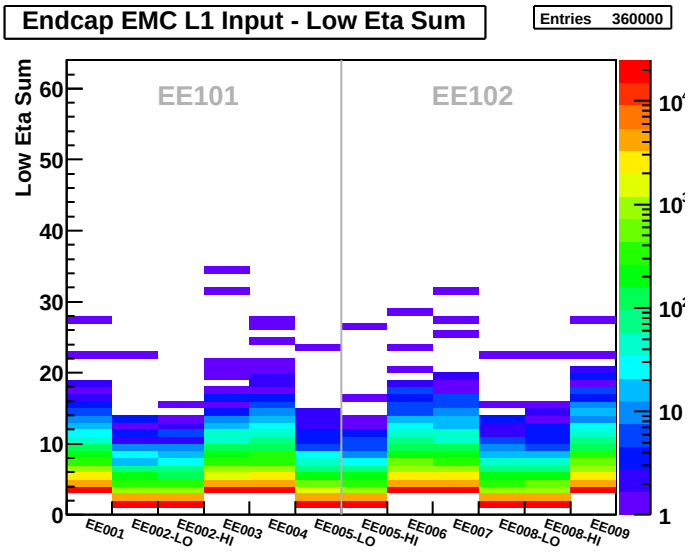

Barrel EMC L1 Input - Low Eta Sum
Entries 0
Low Eta Sum - Simulated
BC101
BC102
BC103
BC104
BC105
BC106
DSM Input Channel

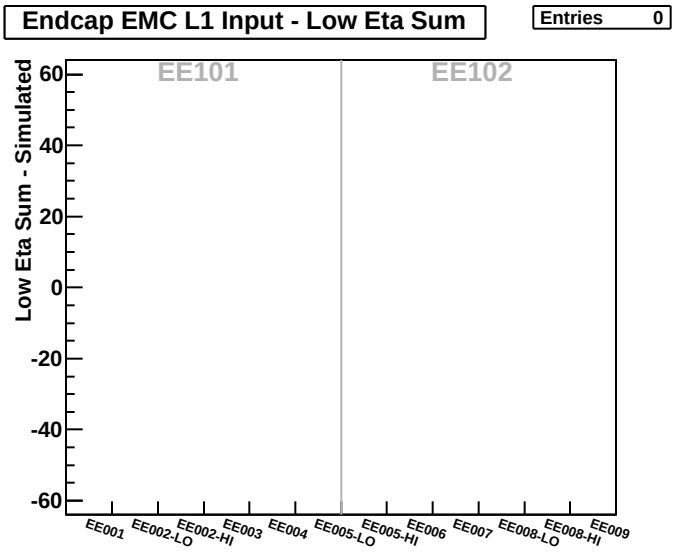

Barrel EMC L1 Input - High Eta Sum
Entries 1080000
High Eta Sum
BC101
BC102
BC103
BC104
BC105
BC106
DSM Input Channel

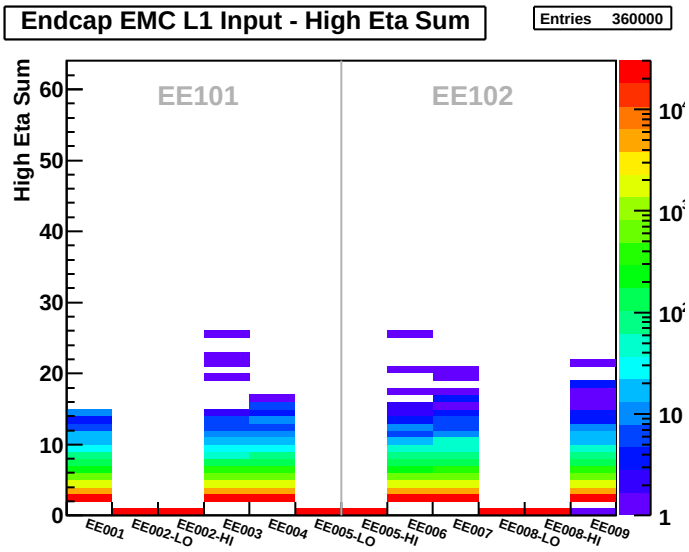

Barrel EMC L1 Input - High Eta Sum
Entries 0
High Eta Sum - Simulated
BC101
BC102
BC103
BC104
BC105
BC106
DSM Input Channel

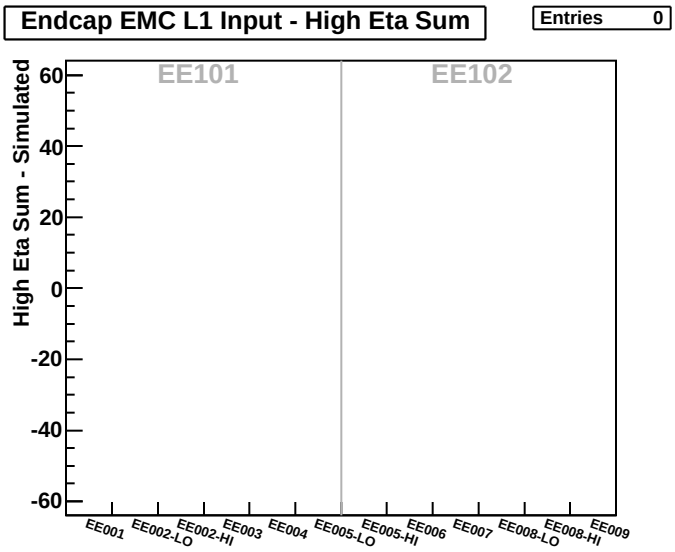

Barrel EMC L1 Input - High Tower Bits
Entries 1080000
High Tower Bits
BC101
BC102
BC103
BC104
BC105
BC106
DSM Input Channel

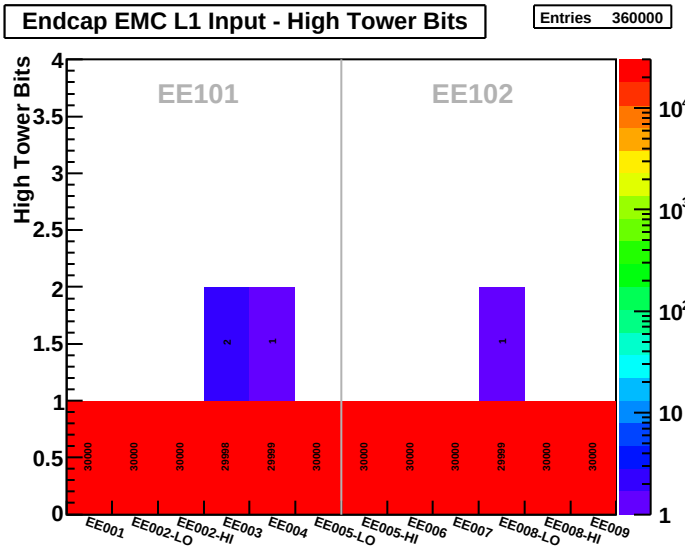

Barrel EMC L1 Input - High Tower Bits
Entries 0
High Tower Bits - Simulated
BC101
BC102
BC103
BC104
BC105
BC106
DSM Input Channel

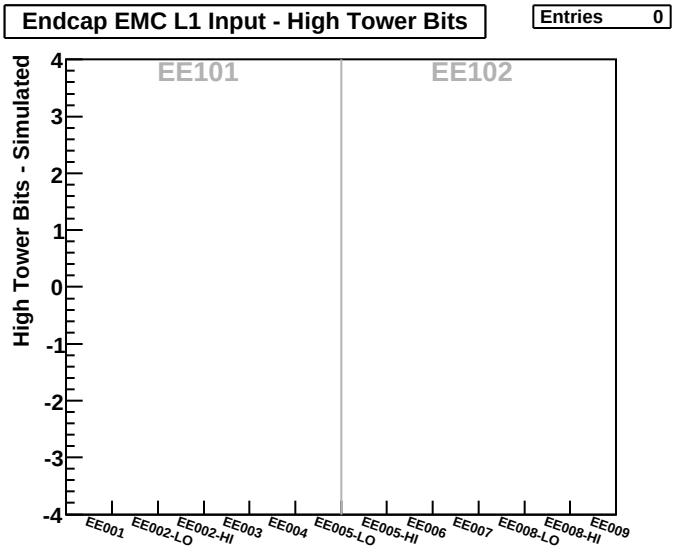

Endcap EMC L1 Input - Low Eta Sum
Entries 360000
Low Eta Sum
EE101
EE102
EE001 EE002-LO EE002-HI EE003 EE004 EE005-LO EE005-HI EE006 EE007 EE008-LO EE008-HI EE009

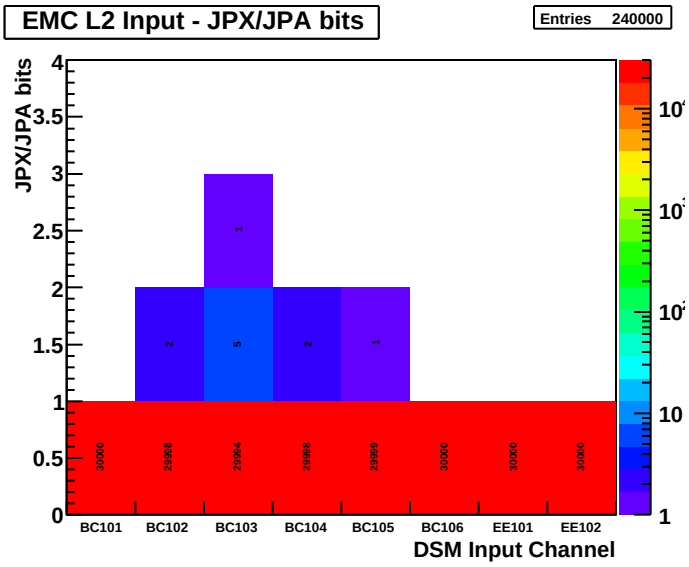

Endcap EMC L1 Input - Low Eta Sum
Entries 0
Low Eta Sum - Simulated
EE101
EE102
EE001 EE002-LO EE002-HI EE003 EE004 EE005-LO EE005-HI EE006 EE007 EE008-LO EE008-HI EE009

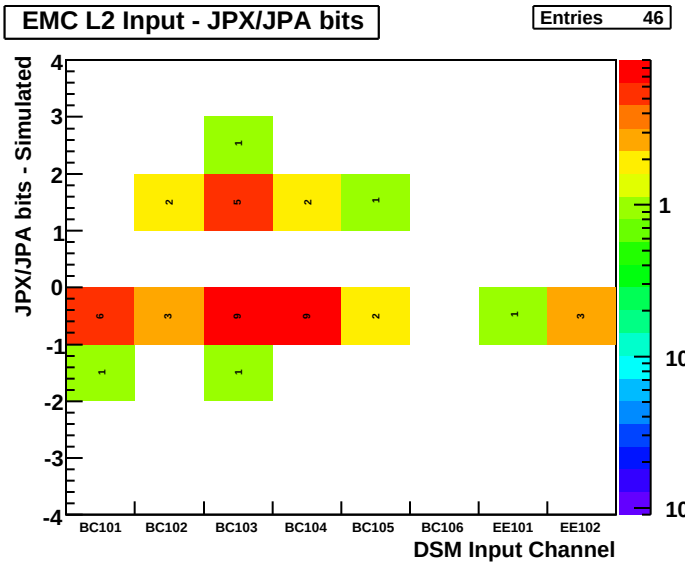

Endcap EMC L1 Input - High Eta Sum
Entries 360000
High Eta Sum
EE101
EE102
EE001 EE002-LO EE002-HI EE003 EE004 EE005-LO EE005-HI EE006 EE007 EE008-LO EE008-HI EE009

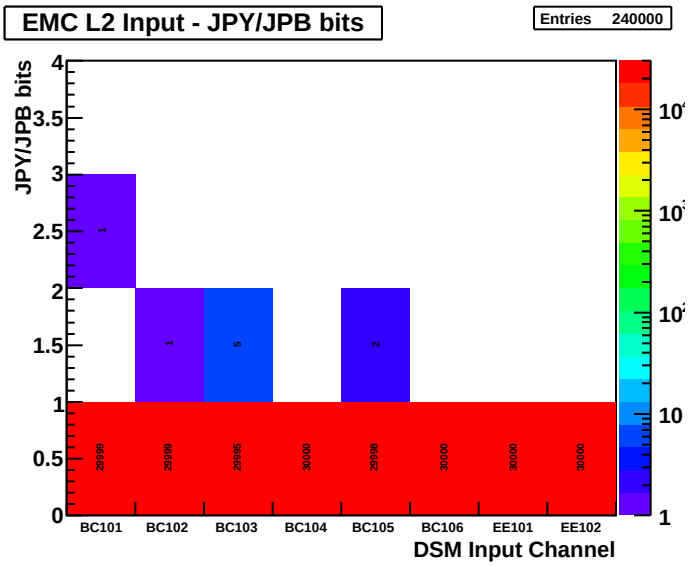

Endcap EMC L1 Input - High Eta Sum
Entries 0
High Eta Sum - Simulated
EE101
EE102
EE001 EE002-LO EE002-HI EE003 EE004 EE005-LO EE005-HI EE006 EE007 EE008-LO EE008-HI EE009

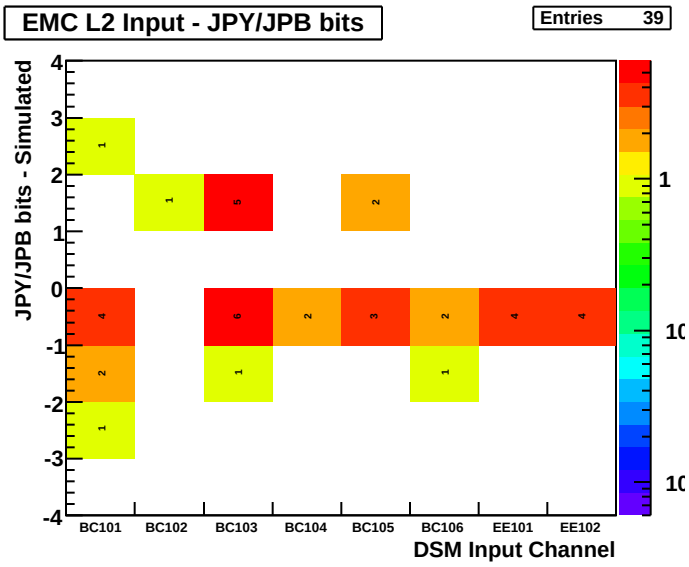

Endcap EMC L1 Input - High Tower Bits
Entries 360000
High Tower Bits
EE101
EE102
EE001 EE002-LO EE002-HI EE003 EE004 EE005-LO EE005-HI EE006 EE007 EE008-LO EE008-HI EE009

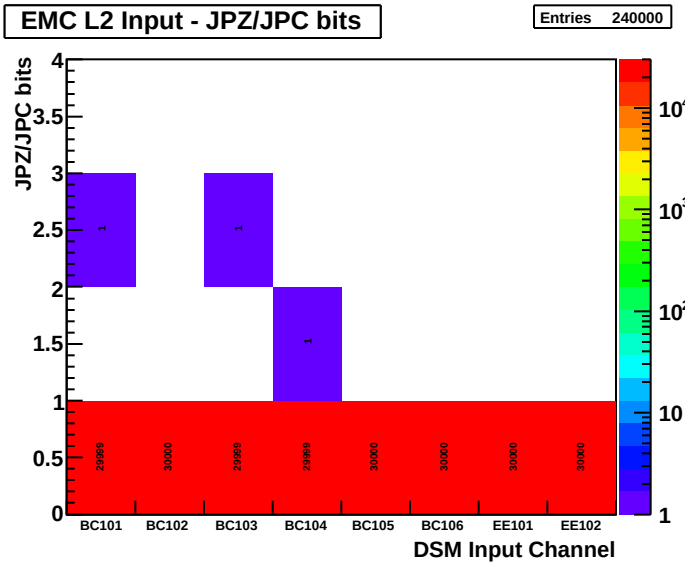

Endcap EMC L1 Input - High Tower Bits
Entries 0
High Tower Bits - Simulated
EE101
EE102
EE001 EE002-LO EE002-HI EE003 EE004 EE005-LO EE005-HI EE006 EE007 EE008-LO EE008-HI EE009

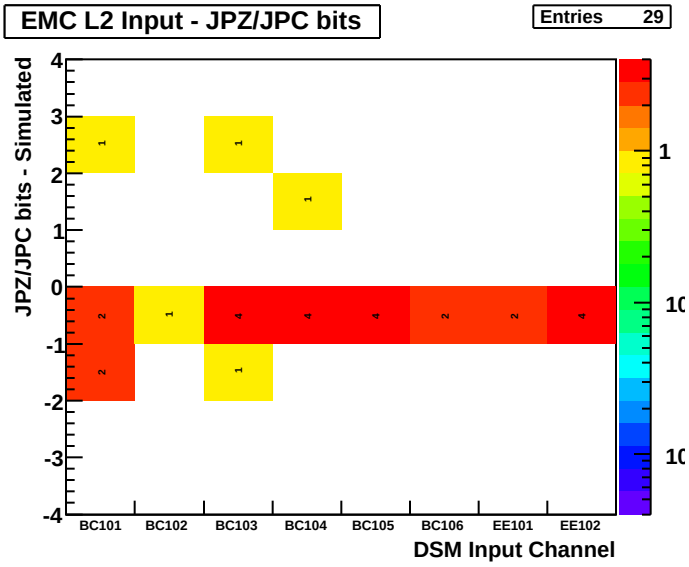

EMC L2 Input - JPX/JPA bits
Entries 240000
JPX/JPA bits
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

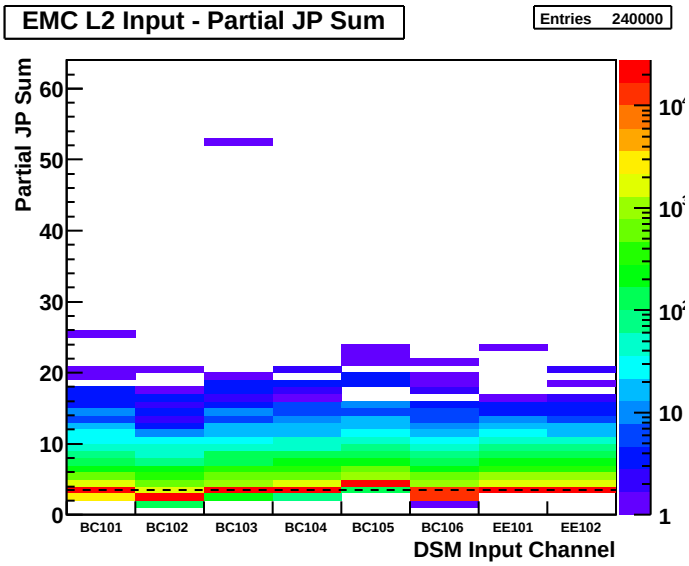

EMC L2 Input - JPX/JPA bits
Entries 46
JPX/JPA bits - Simulated
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

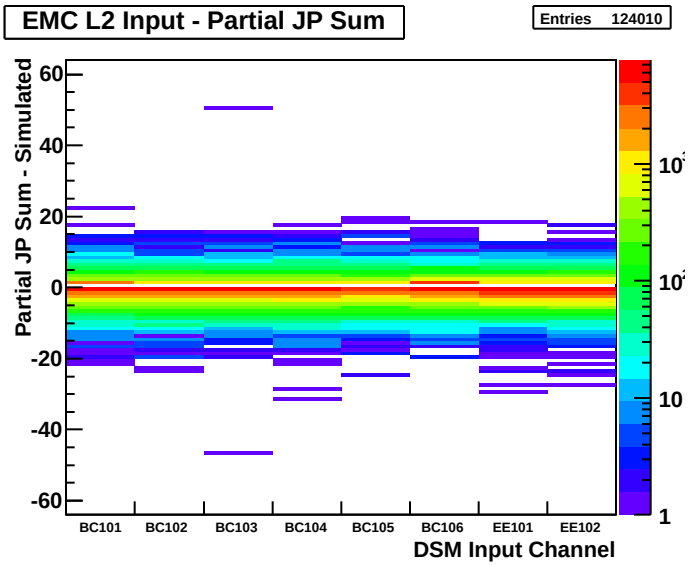

EMC L2 Input - JPY/JPB bits
Entries 240000
JPY/JPB bits
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

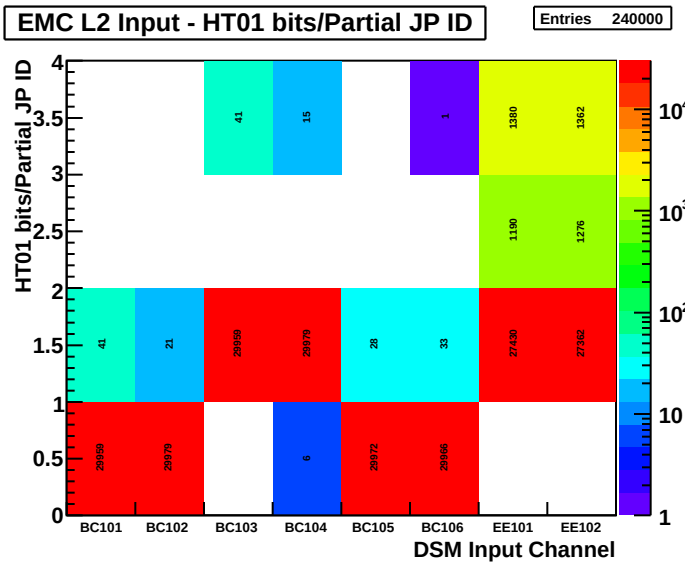

EMC L2 Input - JPY/JPB bits
Entries 39
JPY/JPB bits - Simulated
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

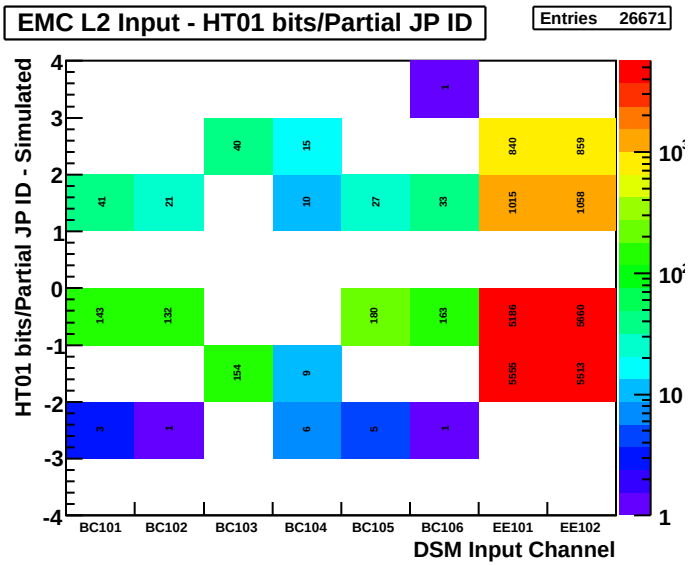

EMC L2 Input - JPZ/JPC bits
Entries 240000
JPZ/JPC bits
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

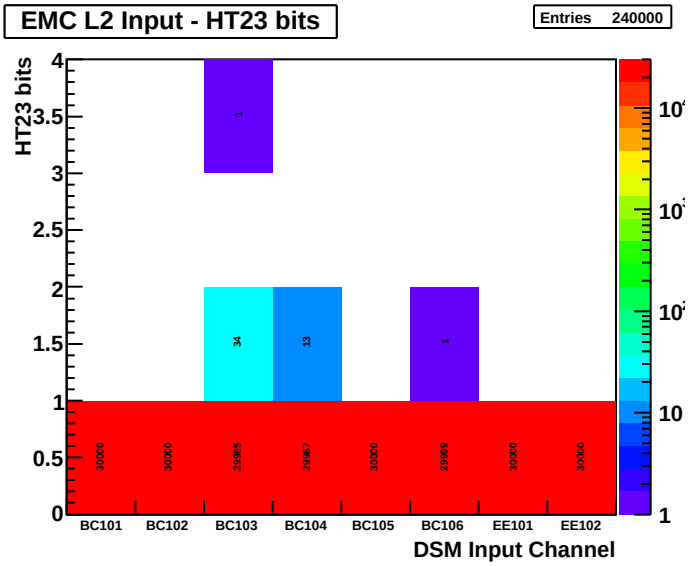

EMC L2 Input - JPZ/JPC bits
Entries 29
JPZ/JPC bits - Simulated
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

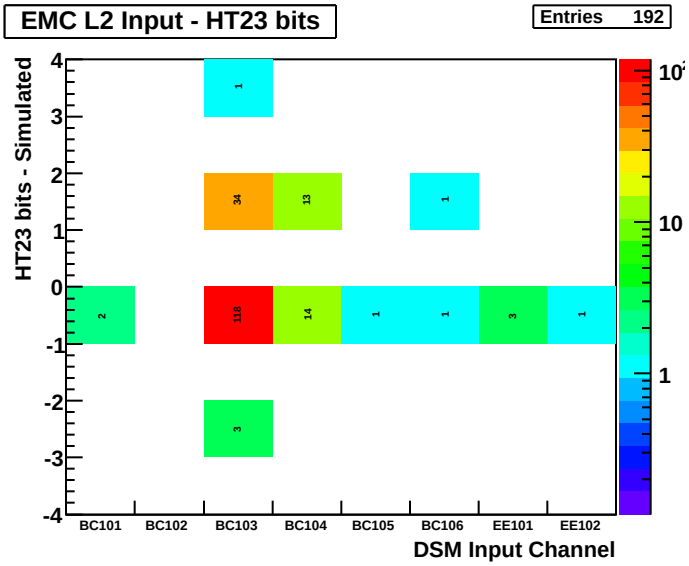

EMC L2 Input - Partial JP Sum
Entries 240000
Partial JP Sum
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

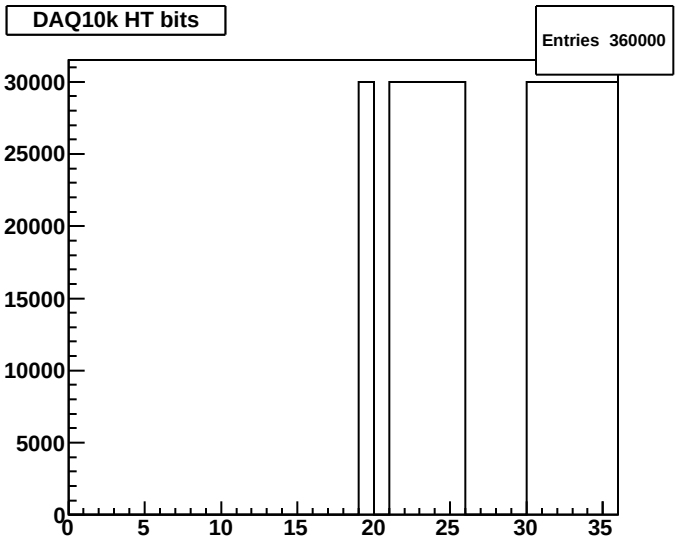

EMC L2 Input - Partial JP Sum
Entries 124010
Partial JP Sum - Simulated
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

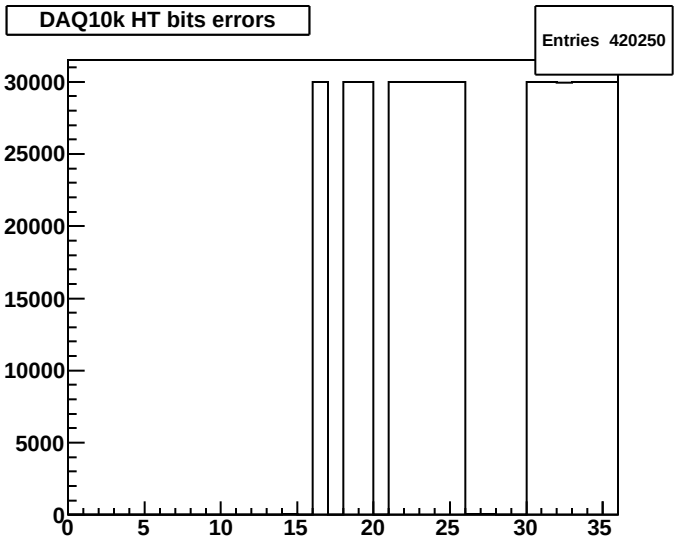

EMC L2 Input - HT01 bits/Partial JP ID
Entries 240000
HT01 bits/Partial JP ID
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

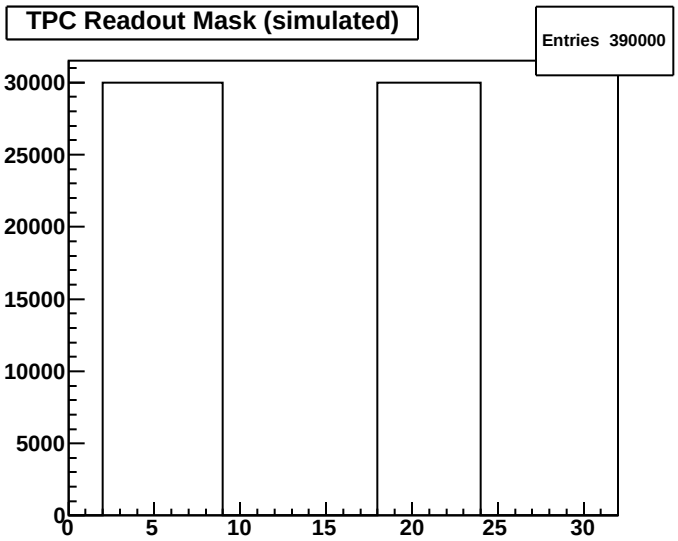

EMC L2 Input - HT01 bits/Partial JP ID
Entries 26671
HT01 bits/Partial JP ID - Simulated
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

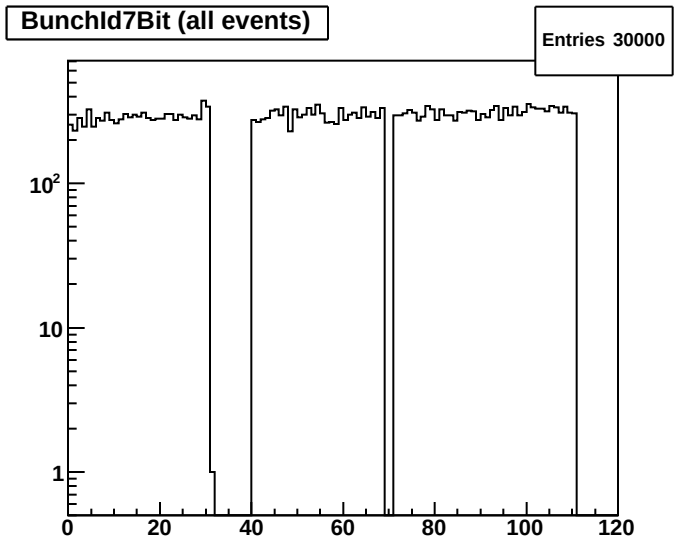

EMC L2 Input - HT23 bits
Entries 240000
HT23 bits
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

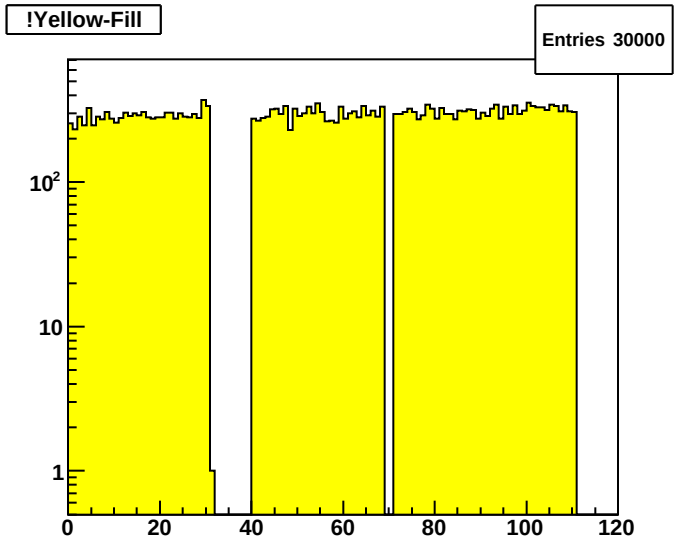

EMC L2 Input - HT23 bits
Entries 192
HT23 bits - Simulated
DSM Input Channel
BC101 BC102 BC103 BC104 BC105 BC106 EE101 EE102

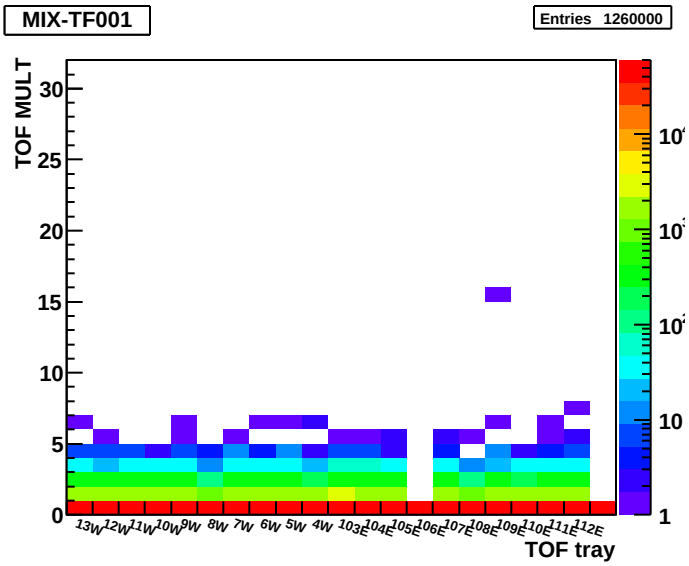

DAQ10k HT bits
Entries 360000
30000
25000
20000
15000
10000
5000
0
0 5 10 15 20 25 30 35

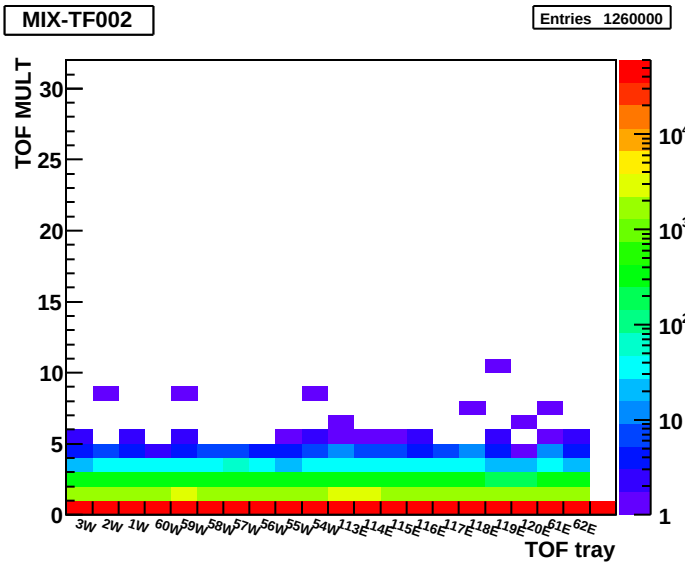

DAQ10k HT bits errors
Entries 420250
30000
25000
20000
15000
10000
5000
0
0 5 10 15 20 25 30 35

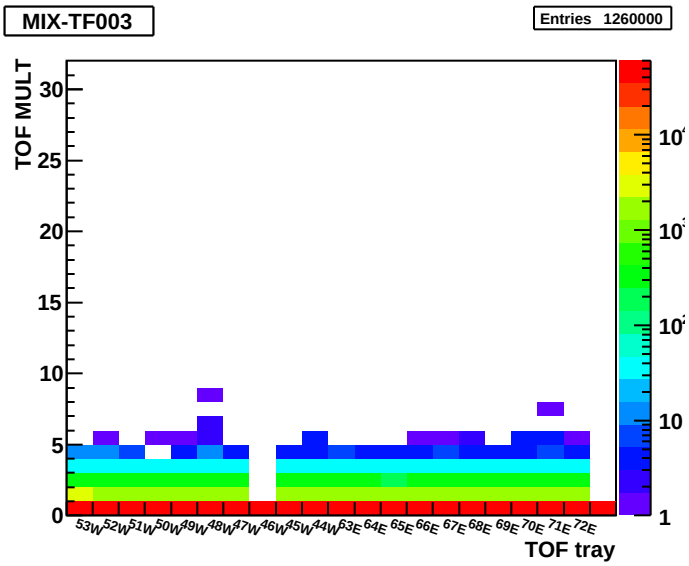

TPC Readout Mask (simulated)
Entries 390000
30000
25000
20000
15000
10000
5000
0
0 5 10 15 20 25 30

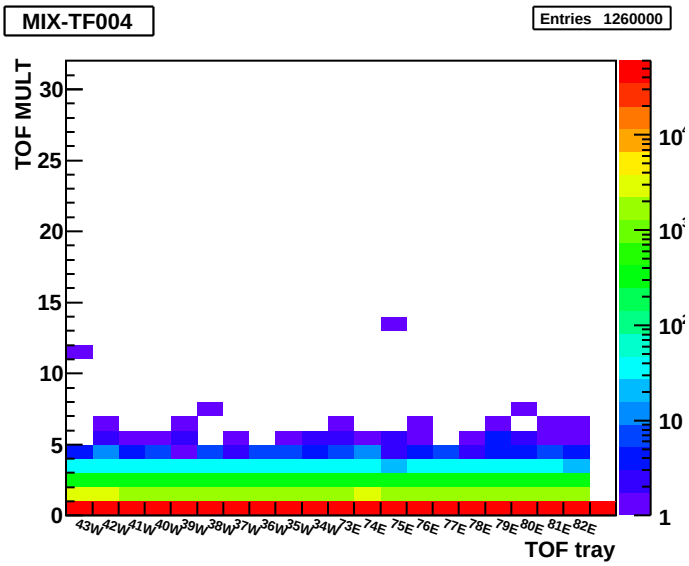

BunchId7Bit (all events)
Entries 30000
10^2
10
1
0 20 40 60 80 100 120

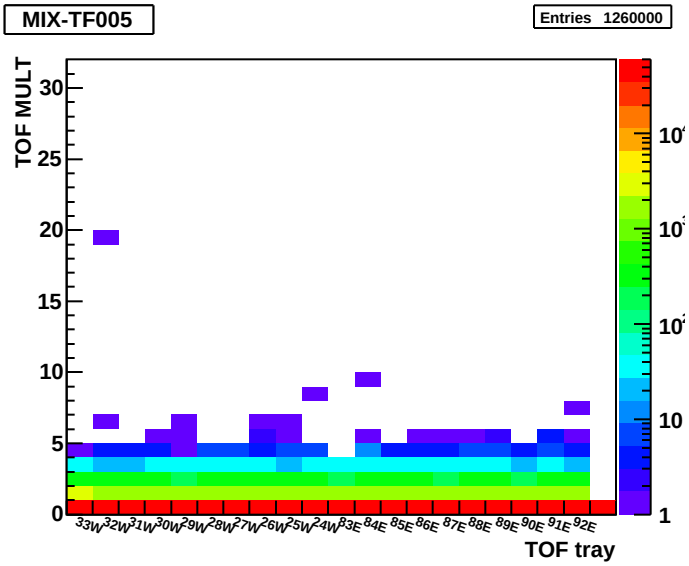

!Yellow-Fill
Entries 30000
10^2
10
1
0 20 40 60 80 100 120

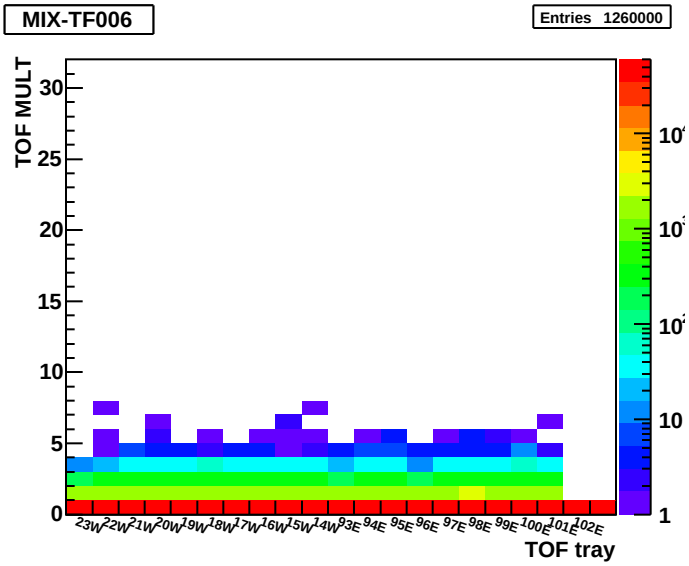

MIX-TF001
Entries 1260000
TOF MULT
TOF tray

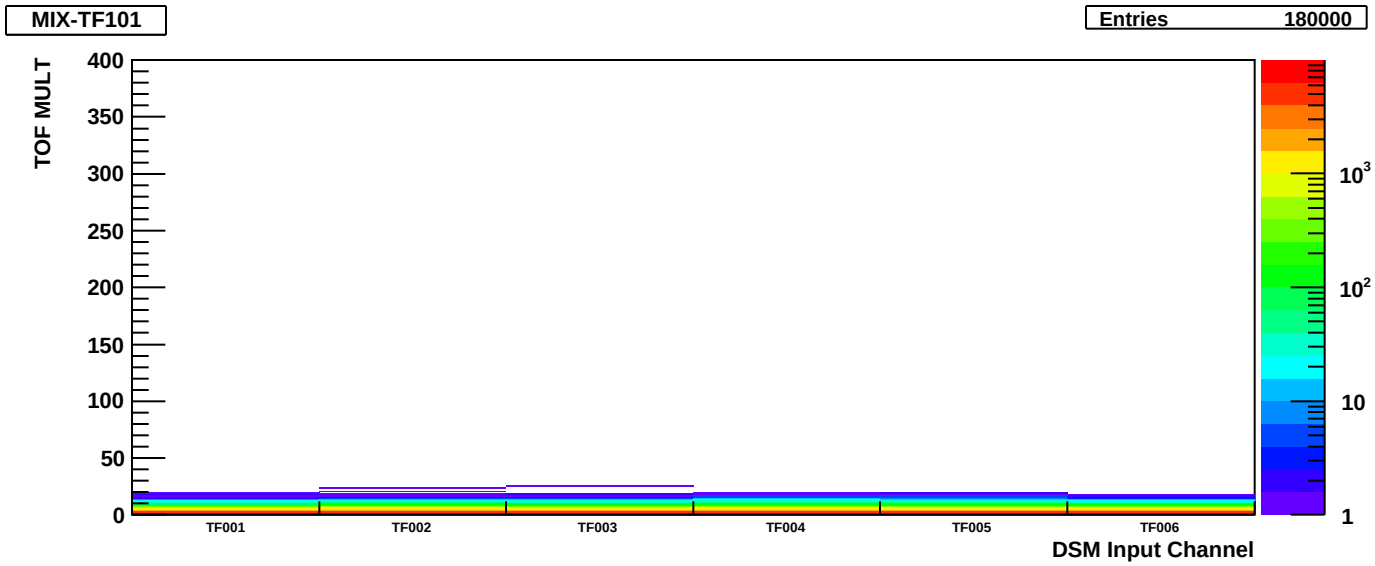

MIX-TF002
Entries 1260000
TOF MULT
TOF tray

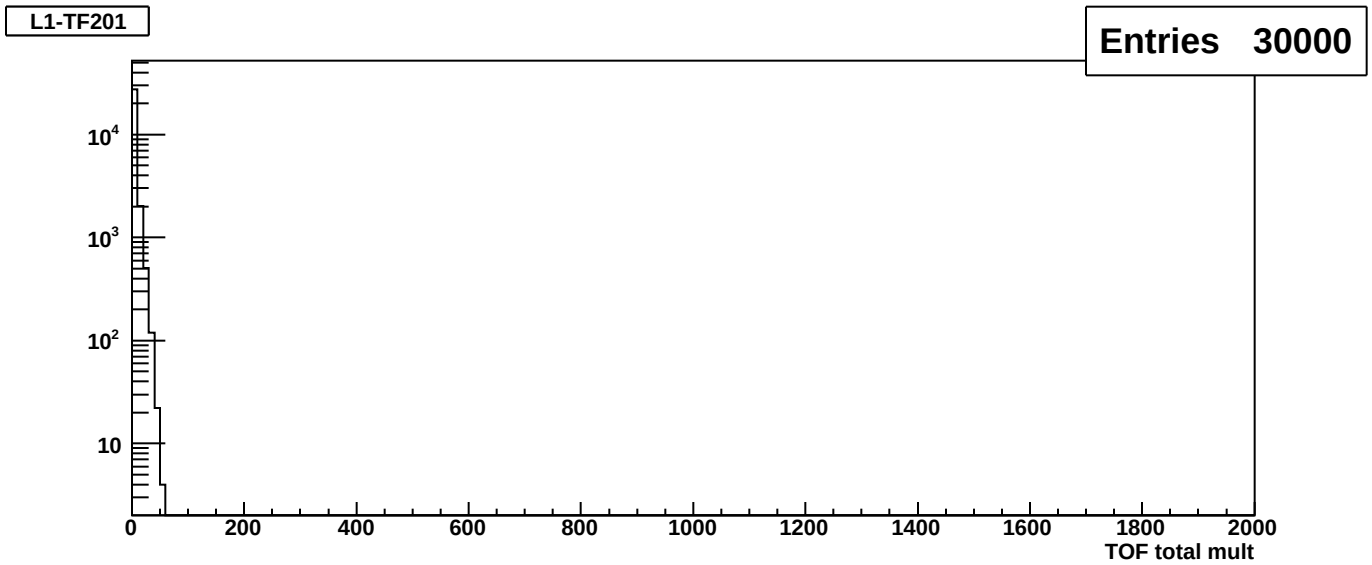

MIX-TF003
Entries 1260000
TOF MULT
TOF tray

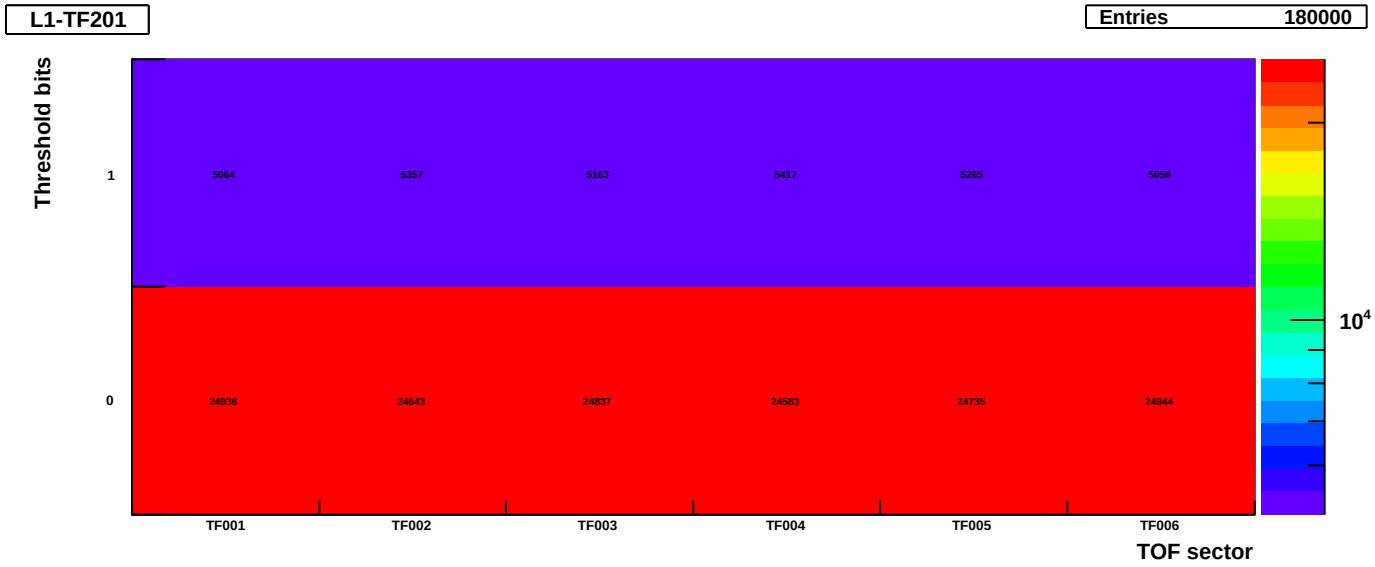

MIX-TF004
Entries 1260000
TOF MULT
TOF tray

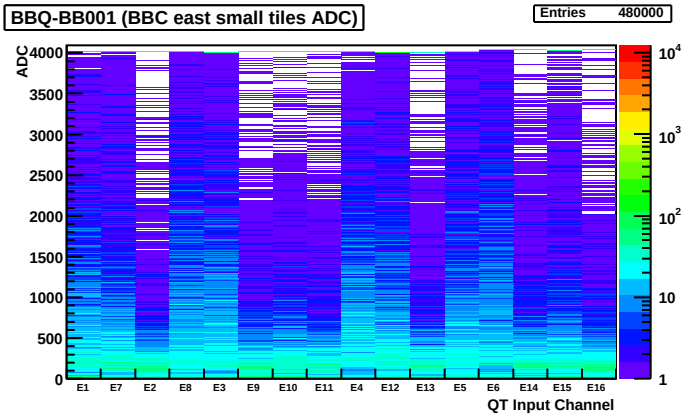

MIX-TF005
Entries 1260000
TOF MULT
TOF tray

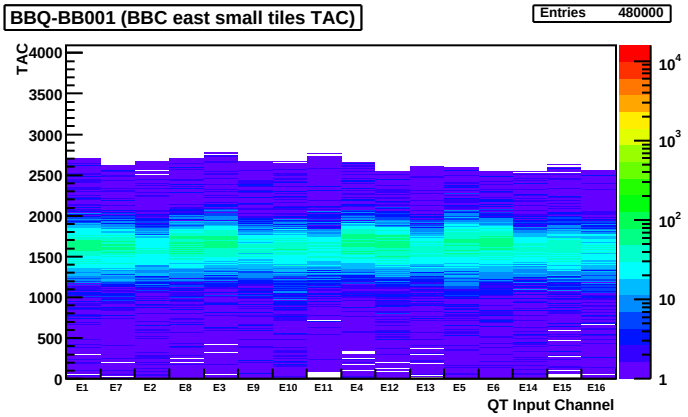

MIX-TF006
Entries 1260000
TOF MULT
TOF tray

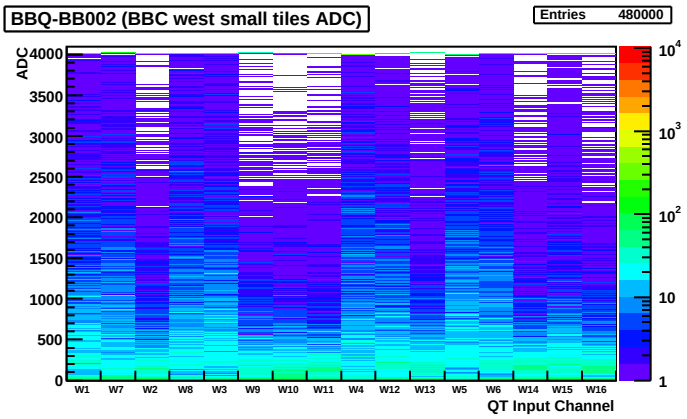

MIX-TF101
Entries 180000
TOF MULT
400
350
300
250
200
150
100
50
0
TF001
TF002
TF003
TF004
TF005
TF006
DSM Input Channel
10^3
10^2
10
1

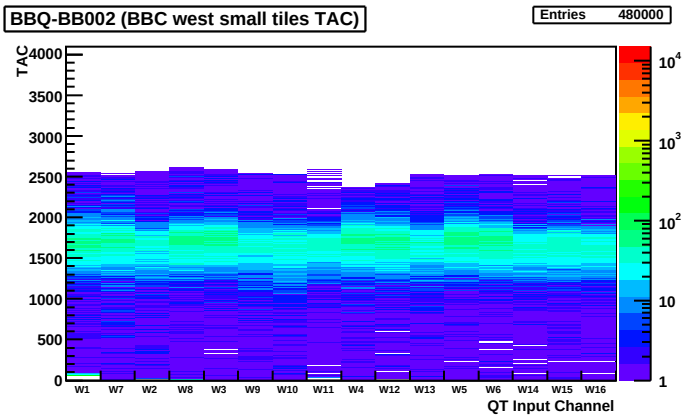

L1-TF201
Entries 30000
10^4
10^3
10^2
10
0
200
400
600
800
1000
1200
1400
1600
1800
2000
TOF total mult

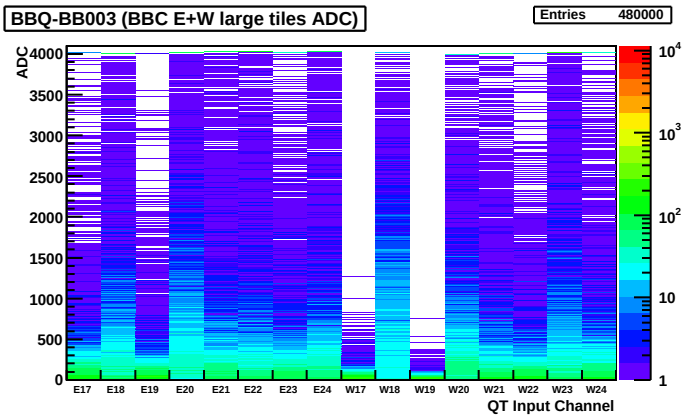

L1-TF201
Entries 180000
Threshold bits
1
0
5064
5357
5163
5417
5265
5056
24936
24643
24837
24583
24735
24944
TF001
TF002
TF003
TF004
TF005
TF006
TOF sector
10^4

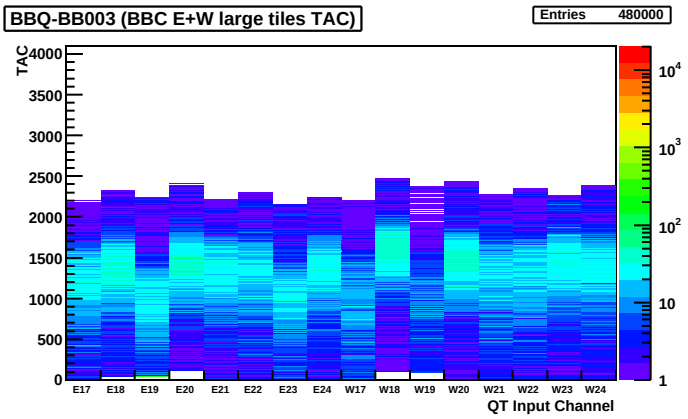

BBQ-BB001 (BBC east small tiles ADC)
Entries 480000
ADC
QT Input Channel

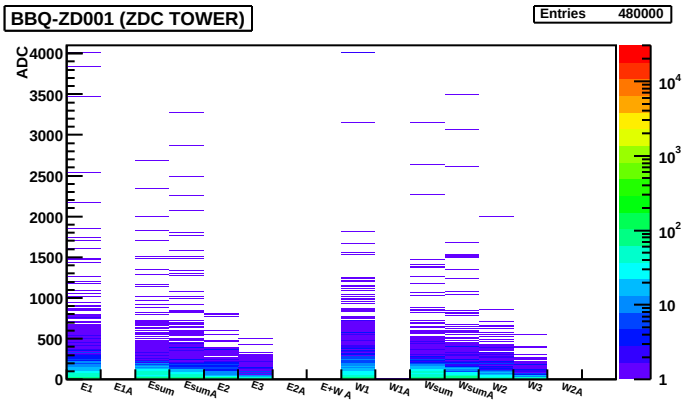

BBQ-BB001 (BBC east small tiles TAC)
Entries 480000
TAC
QT Input Channel

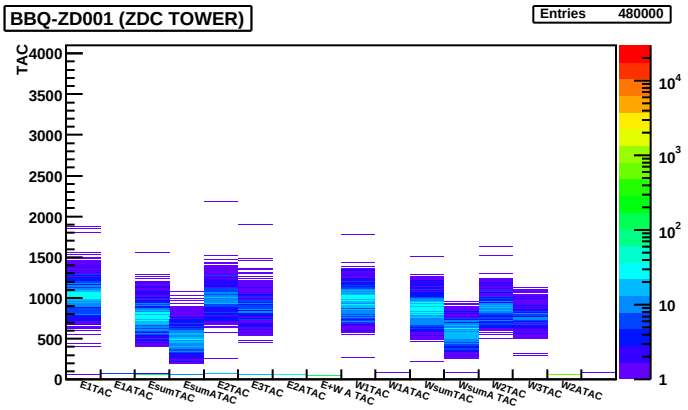

BBQ-BB002 (BBC west small tiles ADC)
Entries 480000
ADC
QT Input Channel

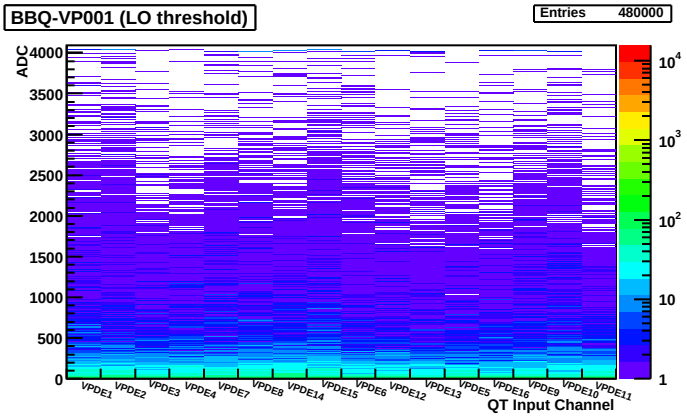

BBQ-BB002 (BBC west small tiles TAC)
Entries 480000
TAC
QT Input Channel

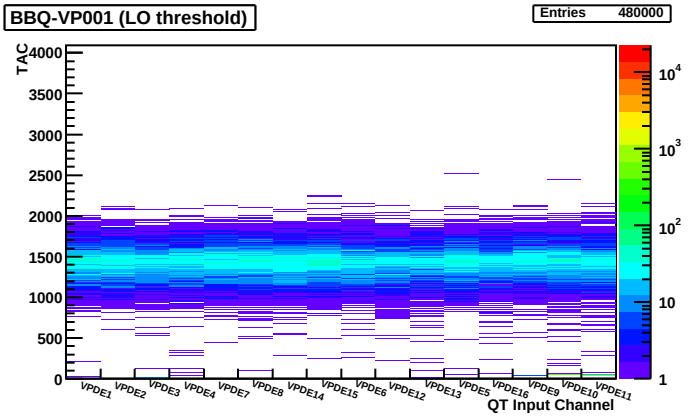

BBQ-BB003 (BBC E+W large tiles ADC)
Entries 480000
ADC
QT Input Channel

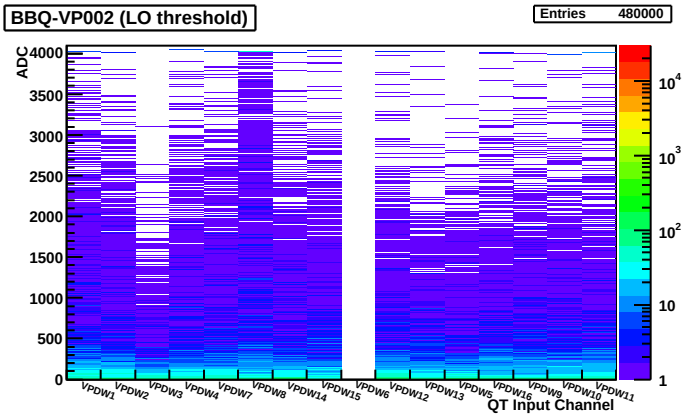

BBQ-BB003 (BBC E+W large tiles TAC)
Entries 480000
TAC
QT Input Channel

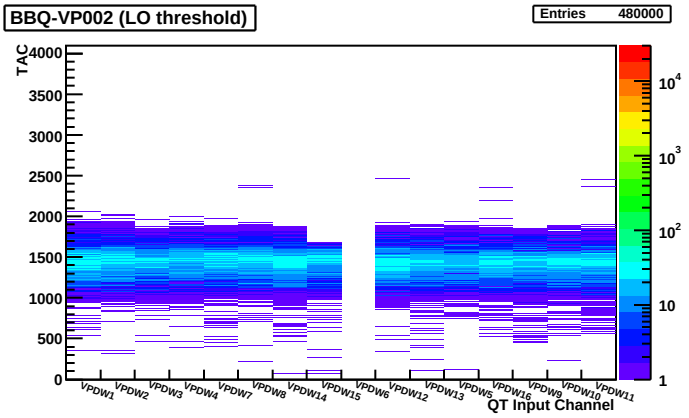

BBQ-ZD001 (ZDC TOWER)
Entries 480000
ADC

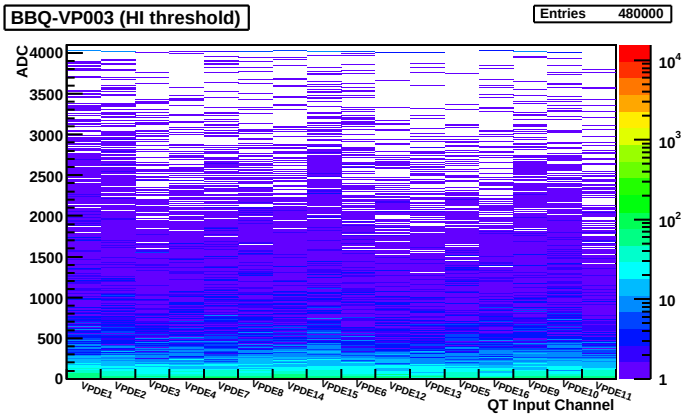

BBQ-ZD001 (ZDC TOWER)
Entries 480000
TAC

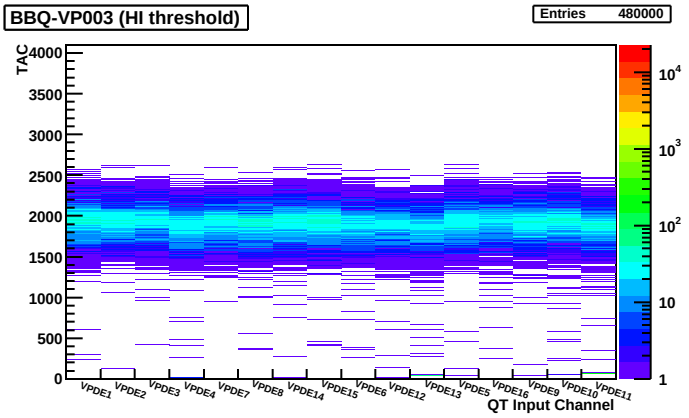

BBQ-VP001 (LO threshold)
Entries 480000
ADC
QT Input Channel

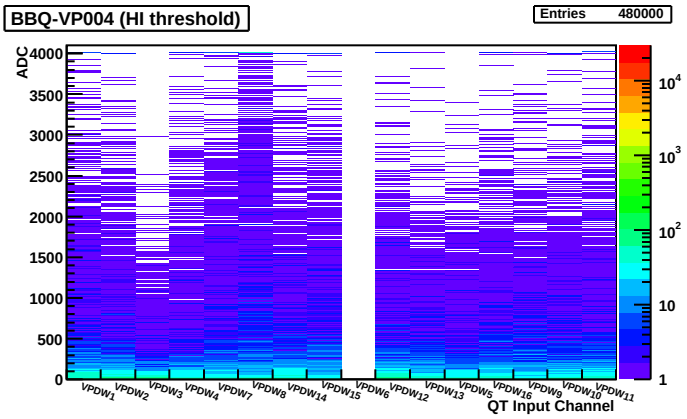

BBQ-VP001 (LO threshold)
Entries 480000
TAC
QT Input Channel

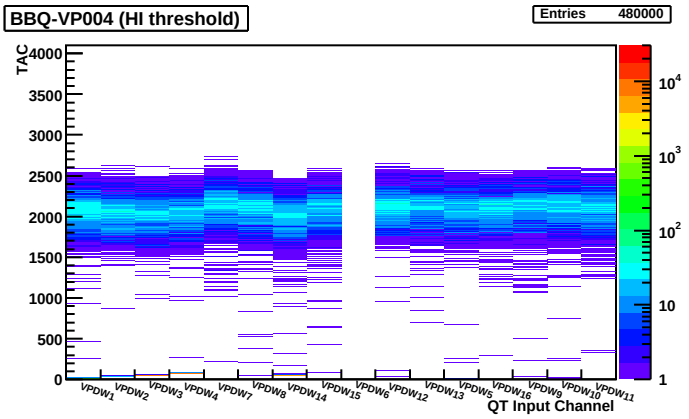

BBQ-VP002 (LO threshold)
Entries 480000
ADC
QT Input Channel

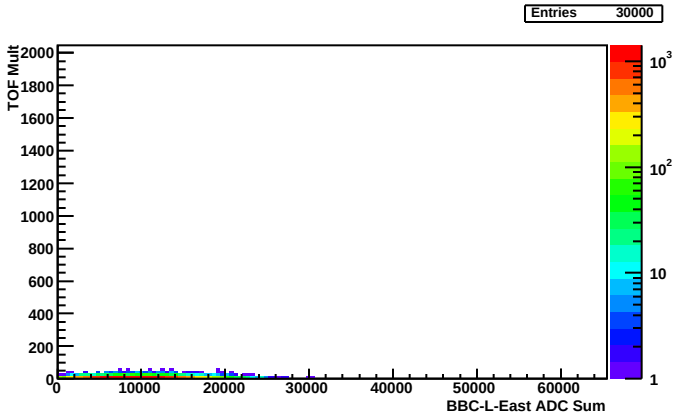

BBQ-VP002 (LO threshold)
Entries 480000
TAC
QT Input Channel

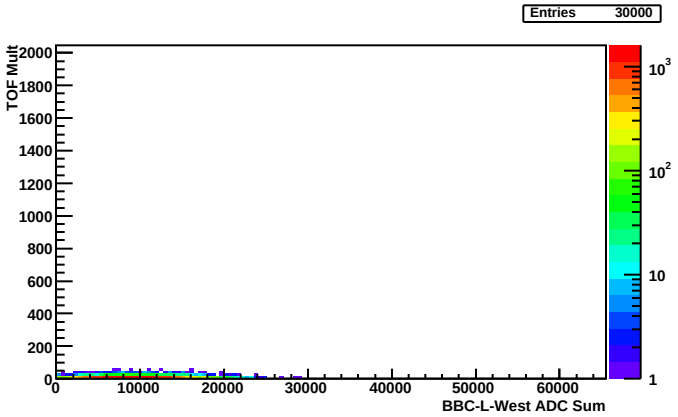

BBQ-VP003 (HI threshold)
Entries 480000
ADC
QT Input Channel

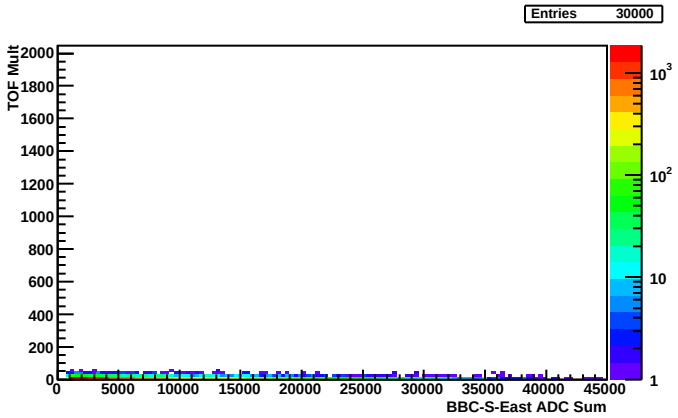

BBQ-VP003 (HI threshold)
Entries 480000
TAC
QT Input Channel

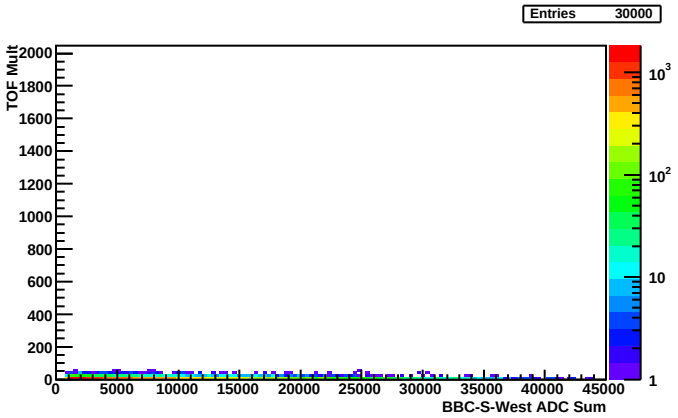

BBQ-VP004 (HI threshold)
Entries 480000
ADC
QT Input Channel

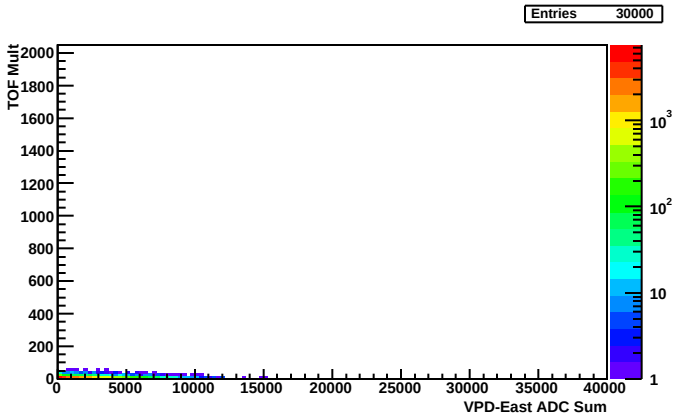

BBQ-VP004 (HI threshold)
Entries 480000
TAC
QT Input Channel

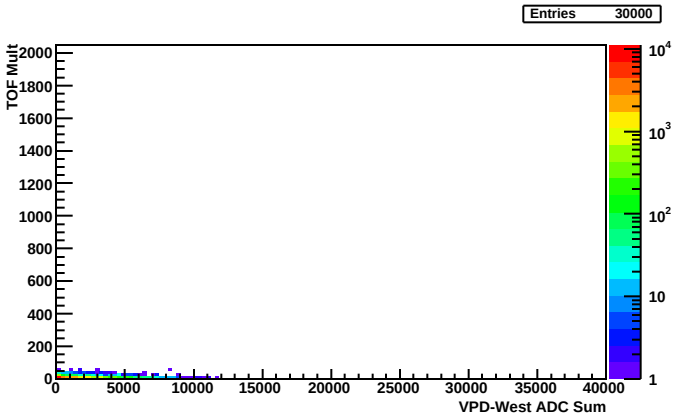

Entries 30000
TOF Mult
BBC-L-East ADC Sum

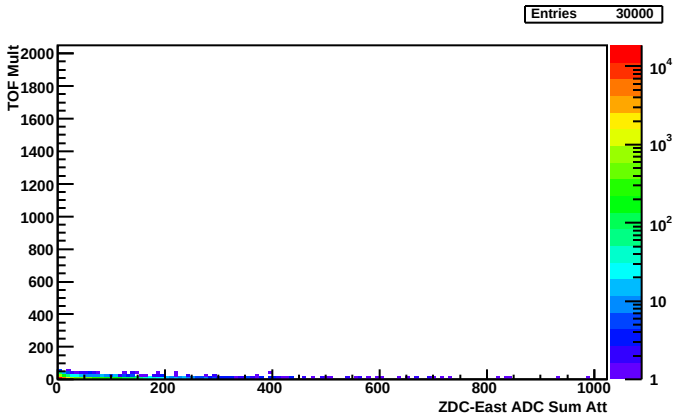

Entries 30000
TOF Mult
BBC-L-West ADC Sum

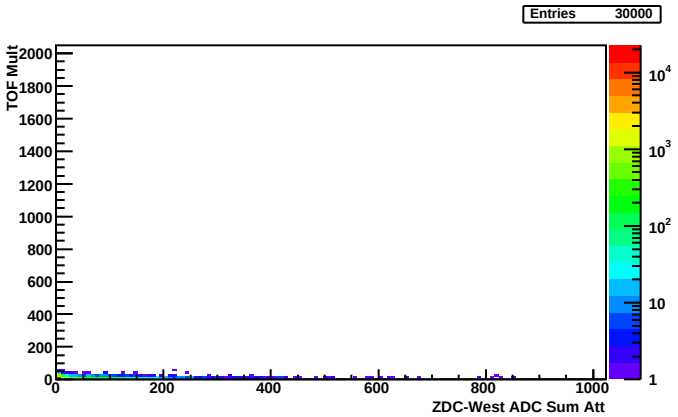

Entries 30000
TOF Mult
BBC-S-East ADC Sum

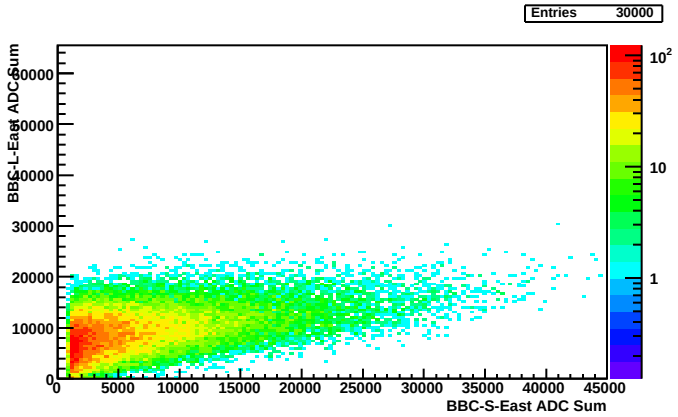

Entries 30000
TOF Mult
BBC-S-West ADC Sum

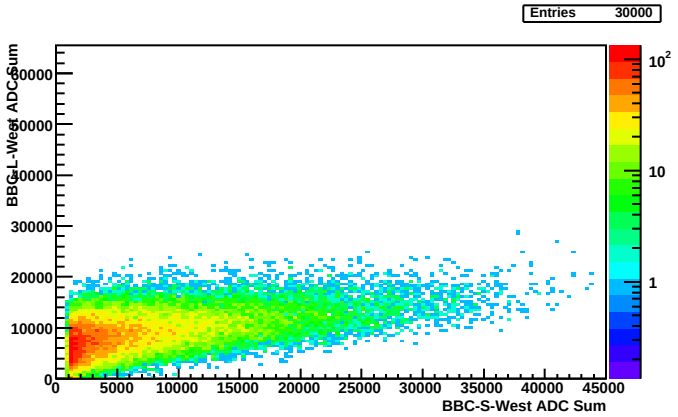

Entries 30000
TOF Mult
VPD-East ADC Sum

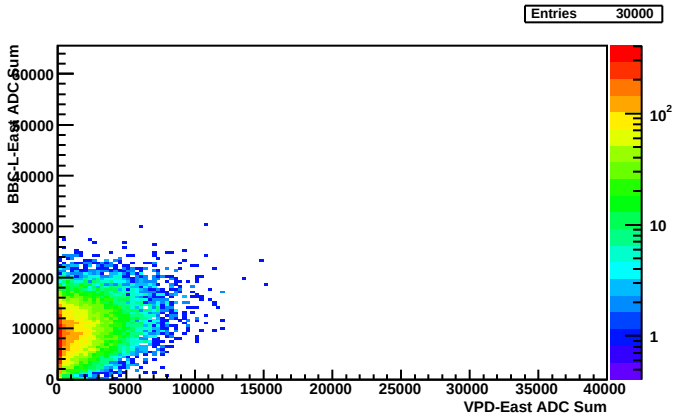

Entries 30000
TOF Mult
VPD-West ADC Sum

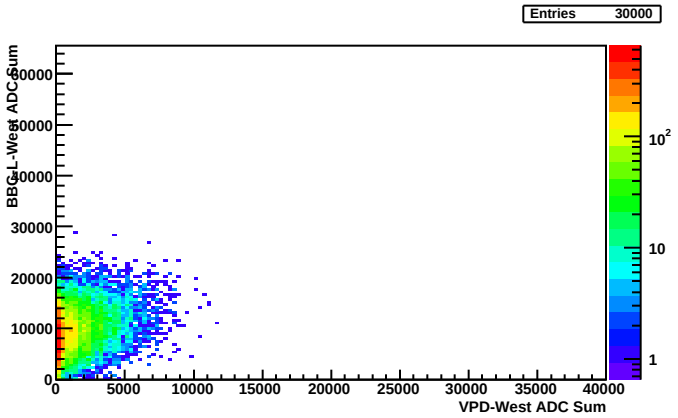

Entries 30000
TOF Mult
ZDC-East ADC Sum Att

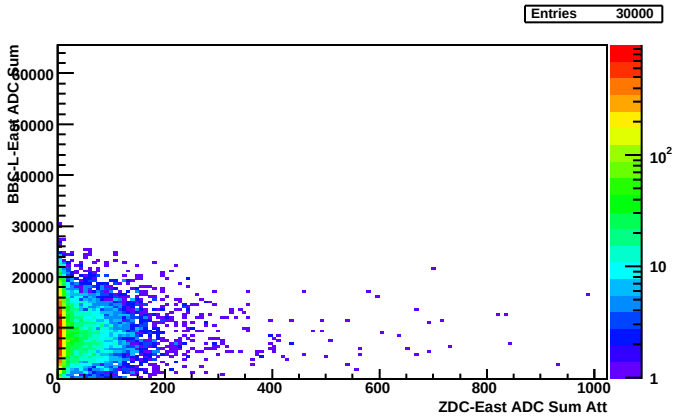

Entries 30000
TOF Mult
ZDC-West ADC Sum Att

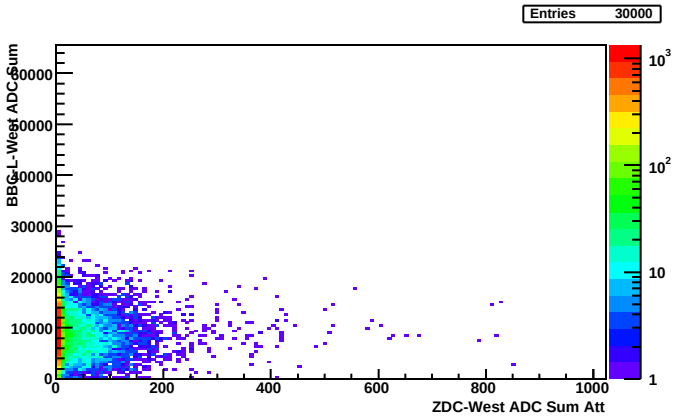

Entries 30000
BBC-L-East ADC Sum
BBC-S-East ADC Sum

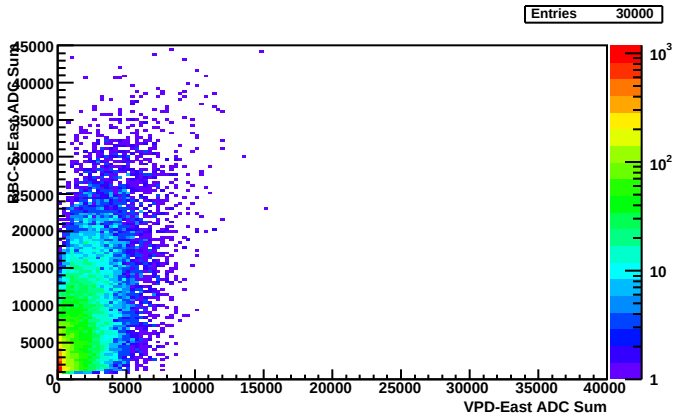

Entries 30000
BBC-L-West ADC Sum
BBC-S-West ADC Sum

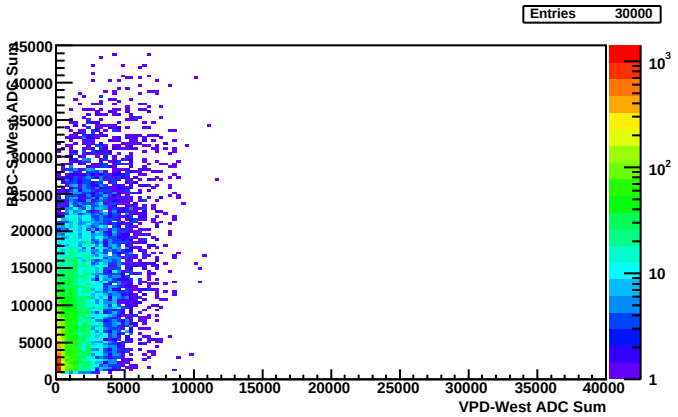

Entries 30000
BBC-L-East ADC Sum
VPD-East ADC Sum

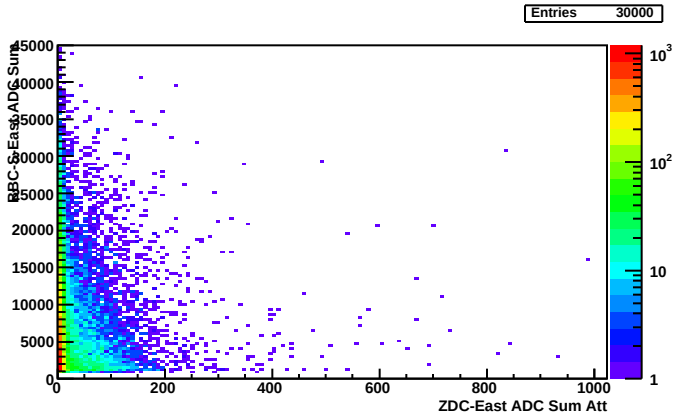

Entries 30000
BBC-L-West ADC Sum
VPD-West ADC Sum

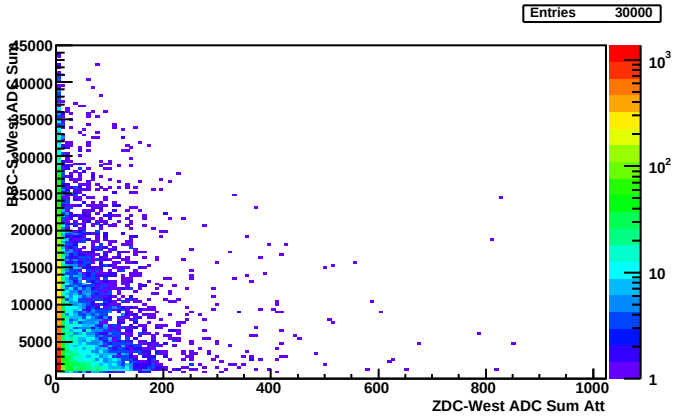

Entries 30000
BBC-L-East ADC Sum
ZDC-East ADC Sum Att

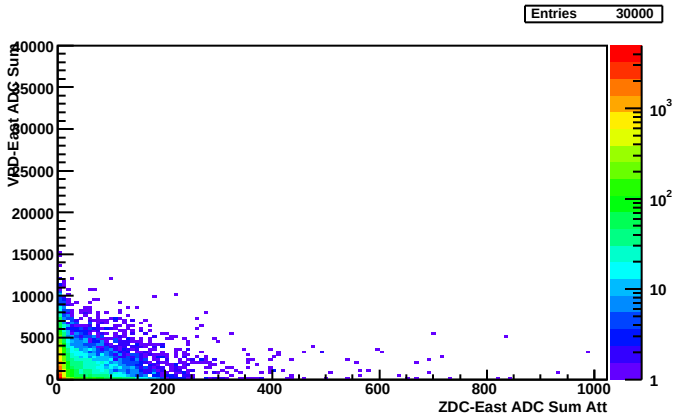

Entries 30000
BBC-L-West ADC Sum
ZDC-West ADC Sum Att

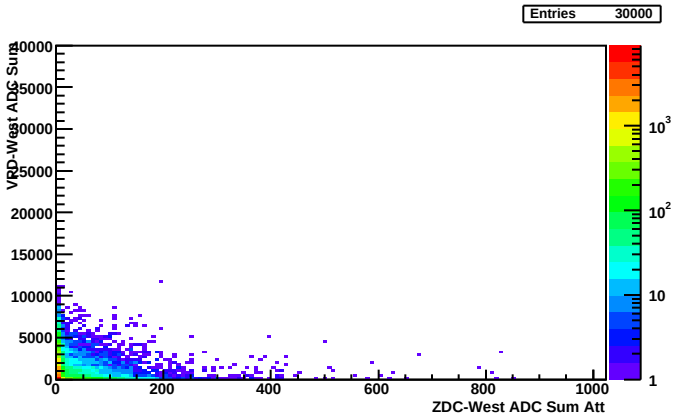

Entries 30000
BBC-S-East ADC Sum
VPD-East ADC Sum

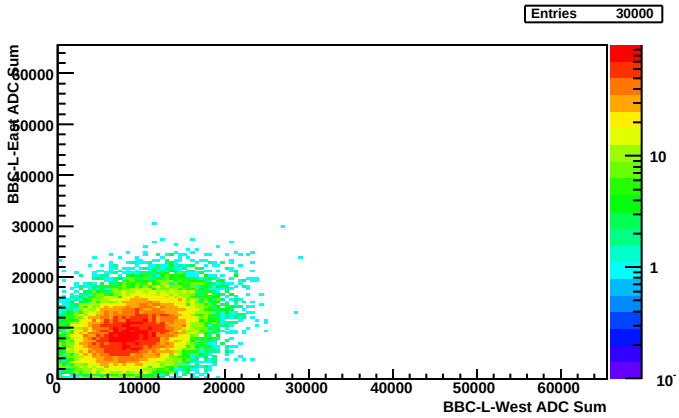

Entries 30000
BBC-S-West ADC Sum
VPD-West ADC Sum

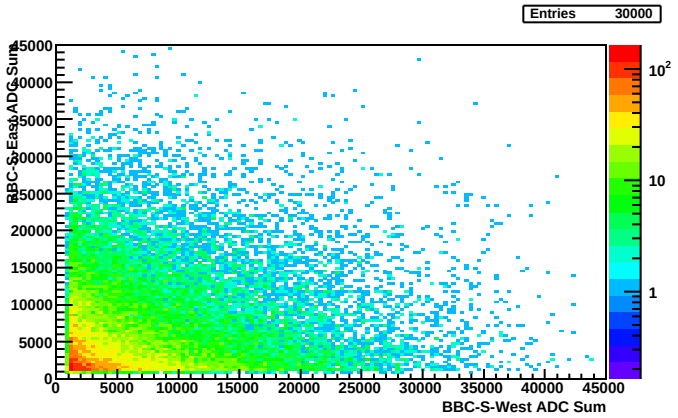

Entries 30000
BBC-S-East ADC Sum
ZDC-East ADC Sum Att

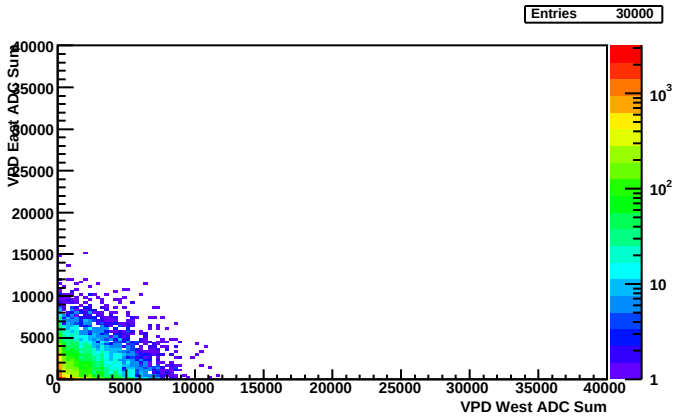

Entries 30000
BBC-S-West ADC Sum
ZDC-West ADC Sum Att

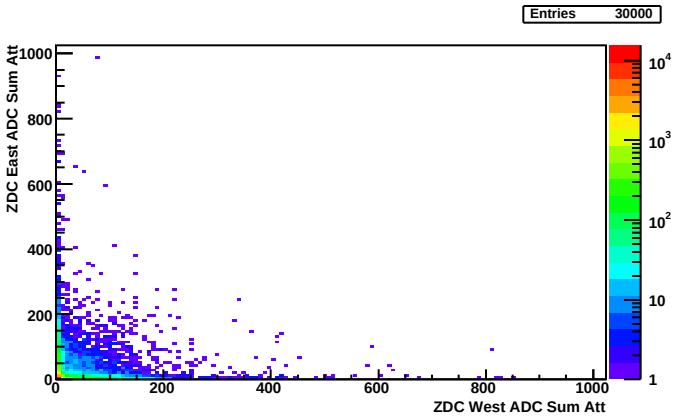

Entries 30000
VPD-East ADC Sum
ZDC-East ADC Sum Att

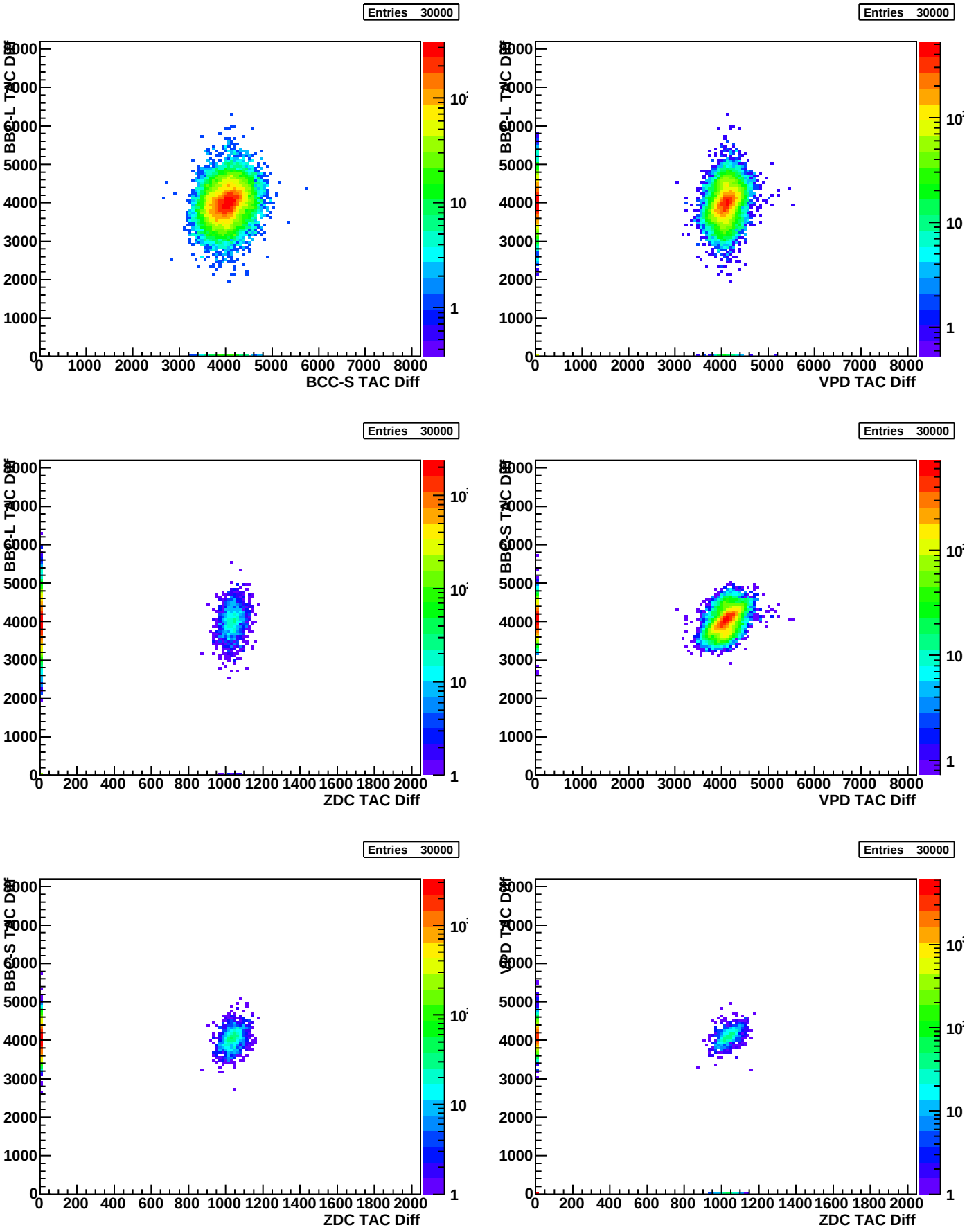

Entries 30000
VPD-West ADC Sum
ZDC-West ADC Sum Att

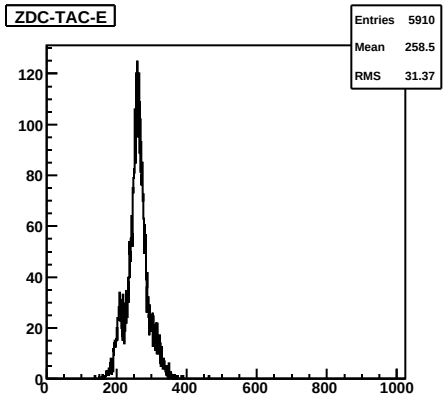

Entries 30000
BBC-L-East ADC Sum
BBC-L-West ADC Sum

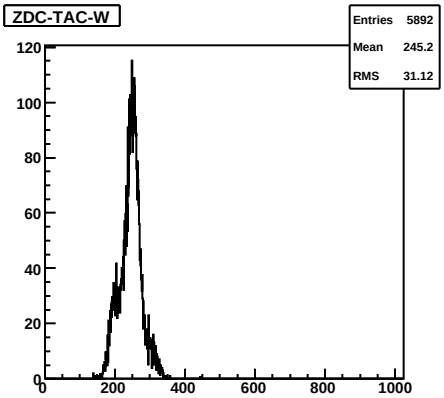

Entries 30000
BBC-S-East ADC Sum
BBC-S-West ADC Sum

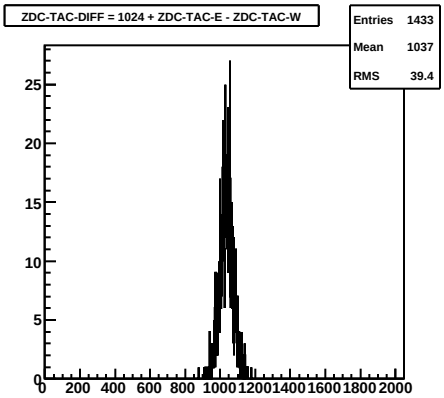

Entries 30000
VPD East ADC Sum
VPD West ADC Sum

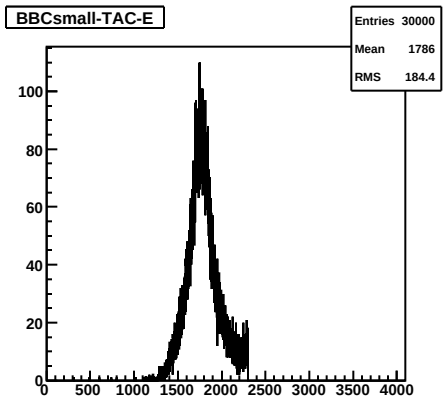

Entries 30000
ZDC East ADC Sum Att
ZDC West ADC Sum Att

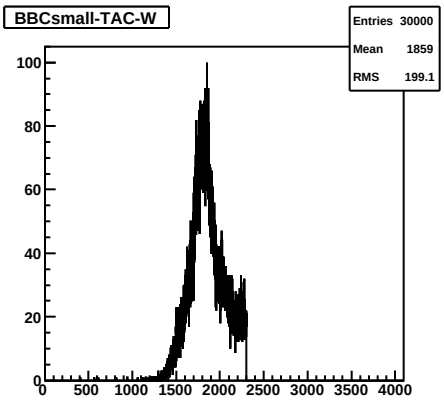

Entries 30000
BBC-L TAC Diff
BCC-S TAC Diff
Entries 30000
BBC-L TAC Diff
VPD TAC Diff
Entries 30000
BBC-L TAC Diff
ZDC TAC Diff
Entries 30000
BBC-S TAC Diff
VPD TAC Diff
Entries 30000
BBC-S TAC Diff
ZDC TAC Diff
Entries 30000
VPD TAC Diff
ZDC TAC Diff

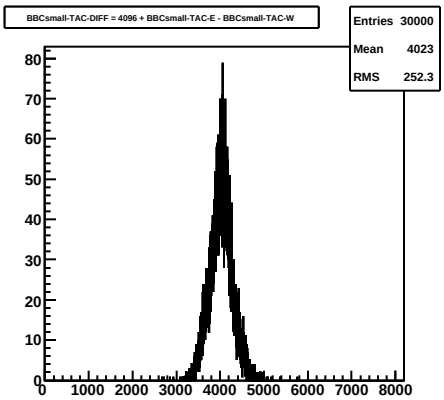

ZDC-TAC-E
Entries 5910
Mean 258.5
RMS 31.37

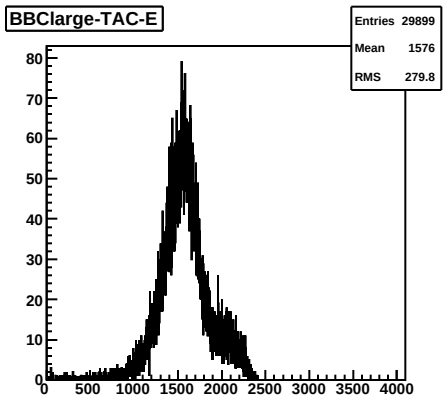

ZDC-TAC-W
Entries 5892
Mean 245.2
RMS 31.12

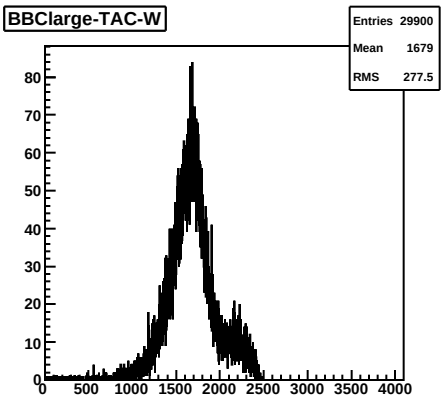

ZDC-TAC-DIFF = 1024 + ZDC-TAC-E - ZDC-TAC-W
Entries 1433
Mean 1037
RMS 39.4

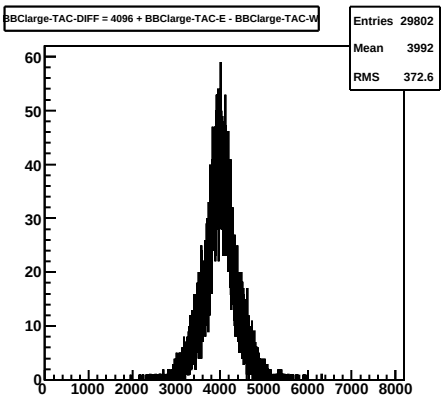

BBCsmall-TAC-E
Entries 30000
Mean 1786
RMS 184.4

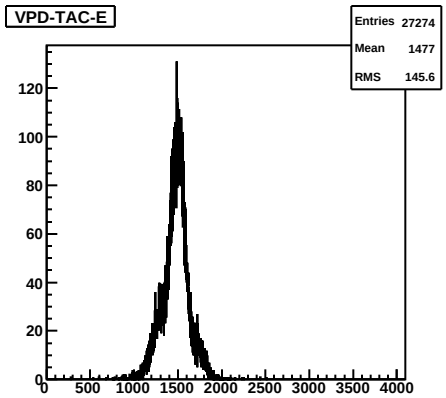

BBCsmall-TAC-W
Entries 30000
Mean 1859
RMS 199.1

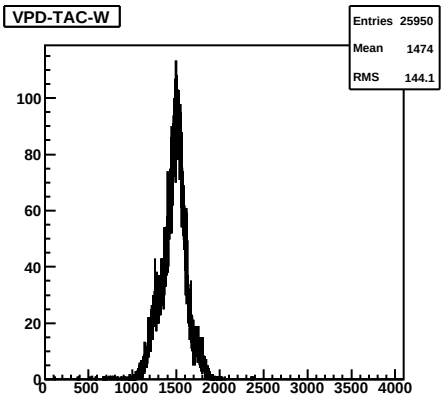

BBCsmall-TAC-DIFF = 4096 + BBCsmall-TAC-E - BBCsmall-TAC-W
Entries 30000
Mean 4023
RMS 252.3

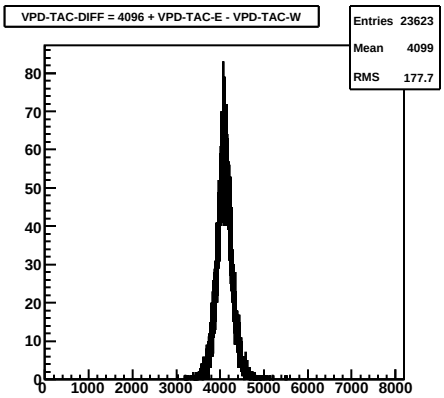

BBClarge-TAC-E
Entries 29899
Mean 1576
RMS 279.8

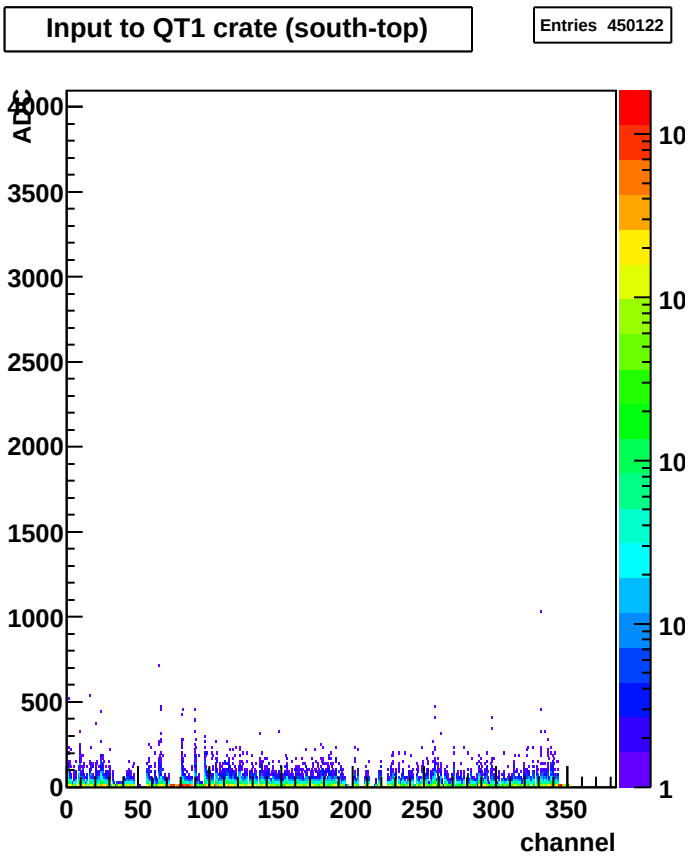

BBClarge-TAC-W
Entries 29900
Mean 1679
RMS 277.5

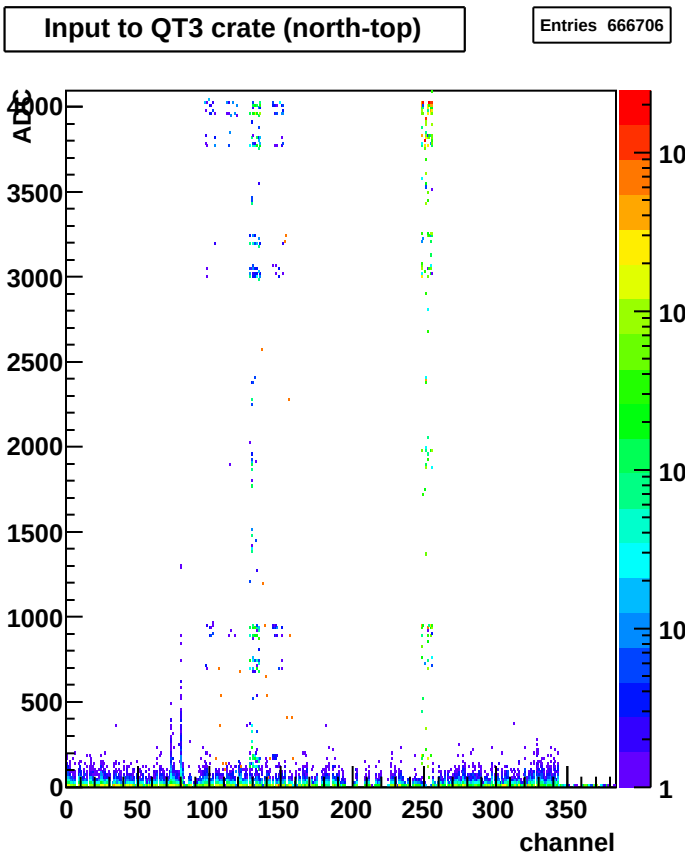

BBClarge-TAC-DIFF = 4096 + BBClarge-TAC-E - BBClarge-TAC-W
Entries 29802
Mean 3992
RMS 372.6

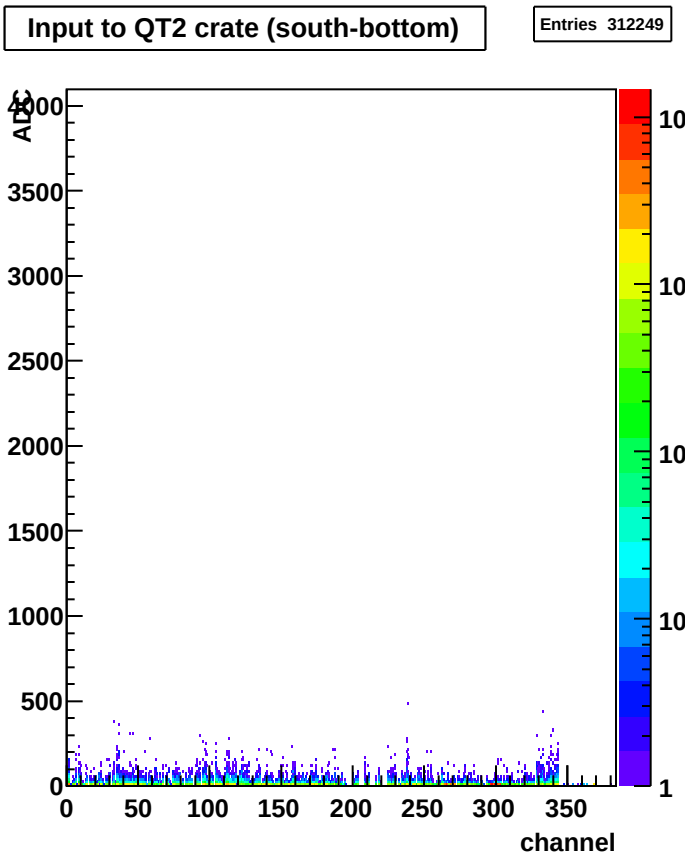

VPD-TAC-E
Entries 27274
Mean 1477
RMS 145.6

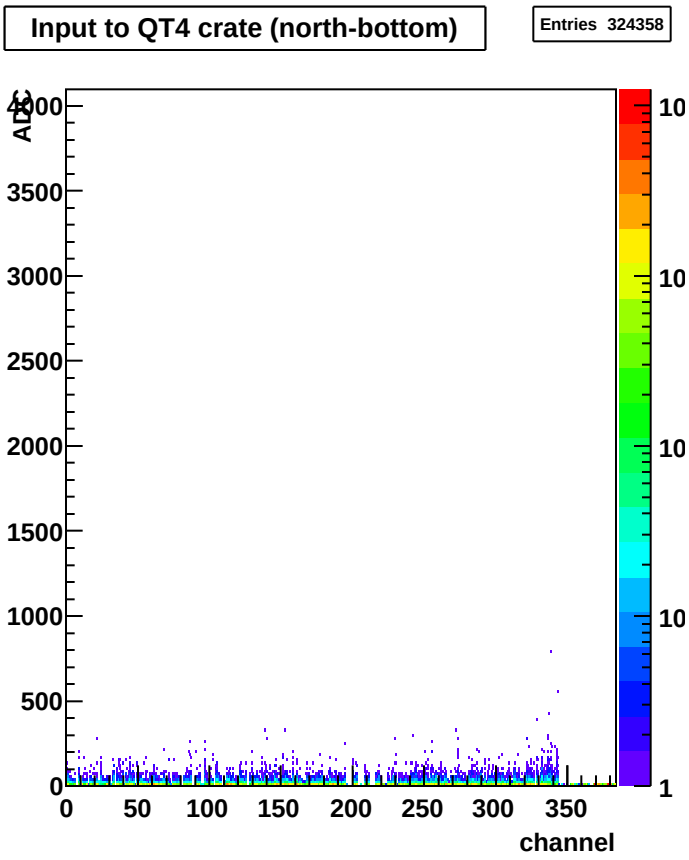

VPD-TAC-W
Entries 25950
Mean 1474
RMS 144.1

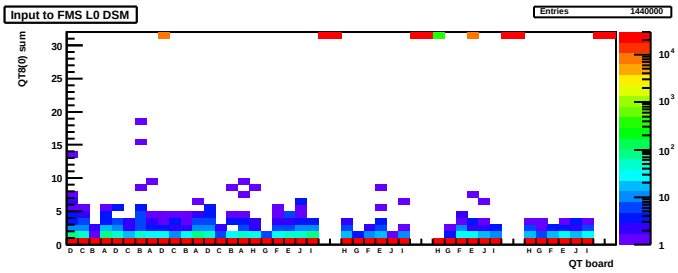

VPD-TAC-DIFF = 4096 + VPD-TAC-E - VPD-TAC-W
Entries 23623
Mean 4099
RMS 177.7

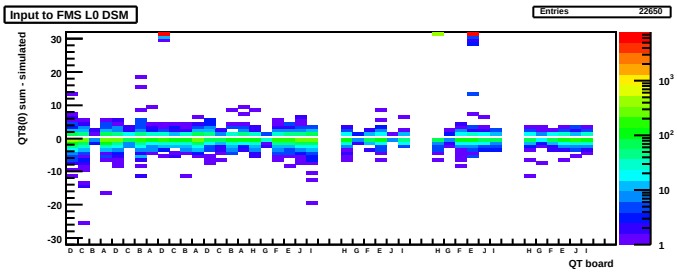

Input to QT1 crate (south-top)
Entries 450122
ADC
channel

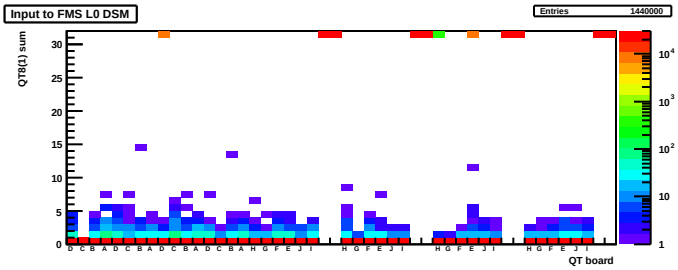

Input to QT3 crate (north-top)
Entries 666706
ADC
channel

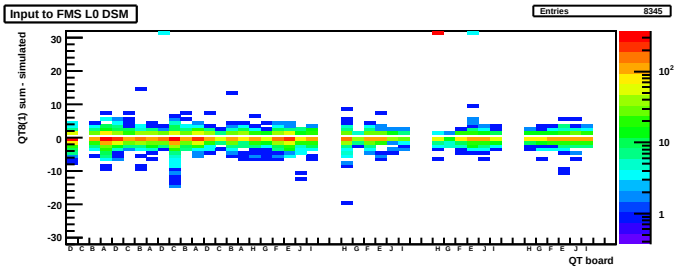

Input to QT2 crate (south-bottom)
Entries 312249
ADC
channel

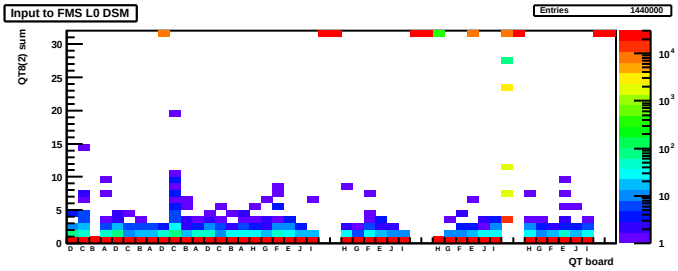

Input to QT4 crate (north-bottom)
Entries 324358
ADC
channel

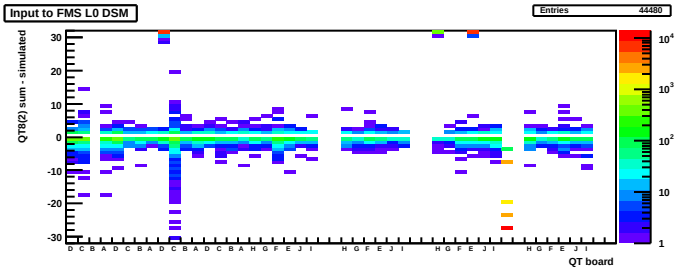

Input to FMS L0 DSM
Entries 1440000
QT8(0) sum
QT board

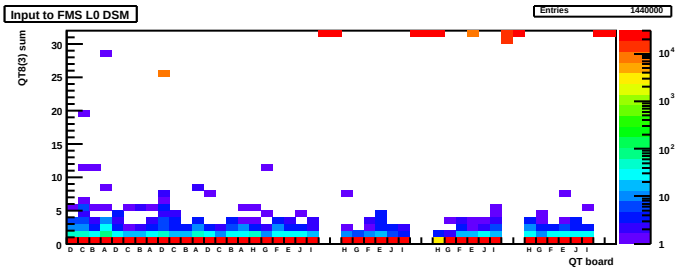

Input to FMS L0 DSM
Entries 22650
QT8(0) sum - simulated
QT board

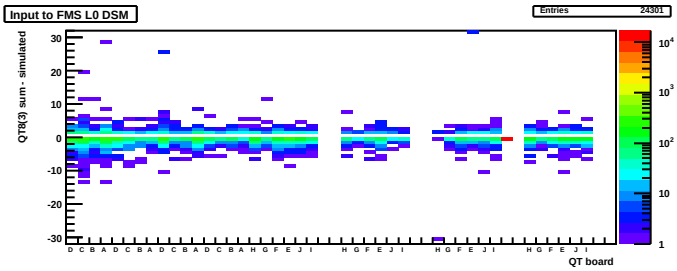

Input to FMS L0 DSM
Entries 1440000
QT8(1) sum
QT board

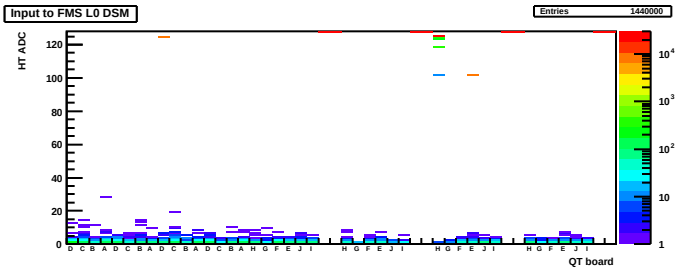

Input to FMS L0 DSM
Entries 8345
QT8(1) sum - simulated
QT board

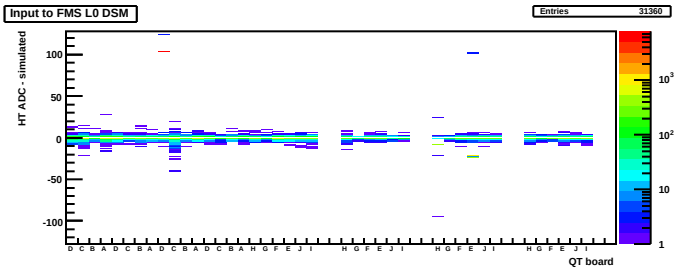

Input to FMS L0 DSM
Entries 1440000
QT8(2) sum
QT board

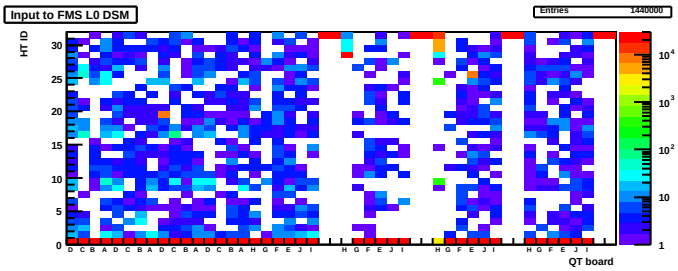

Input to FMS L0 DSM
Entries 44480
QT8(2) sum - simulated
QT board

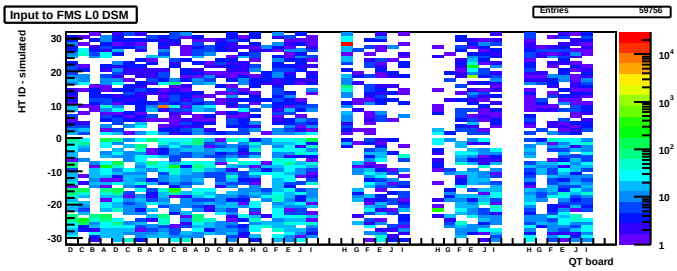

Input to FMS L0 DSM
Entries 1440000
QT8(3) sum
QT board

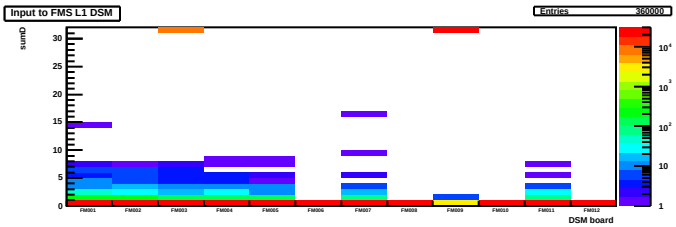

Input to FMS L0 DSM
Entries 24301
QT8(3) sum - simulated
QT board

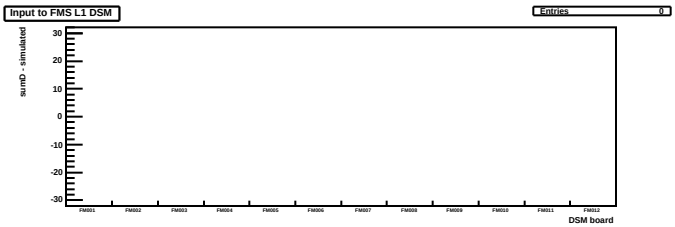

Input to FMS L0 DSM
Entries 1440000
HT ADC
QT board

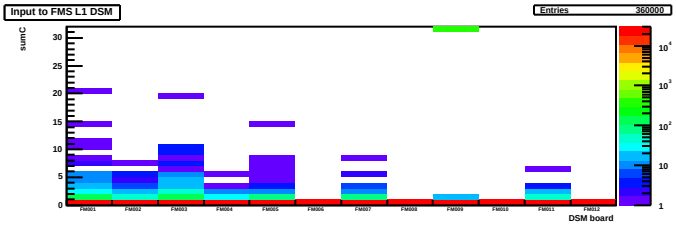

Input to FMS L0 DSM
Entries 31360
HT ADC - simulated
QT board

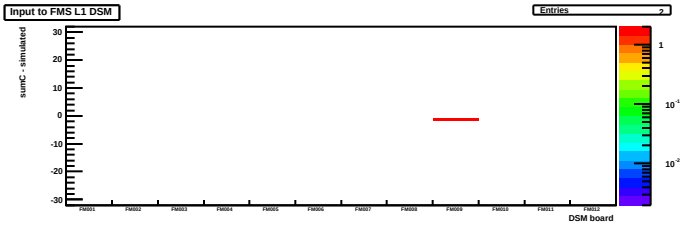

Input to FMS L0 DSM
Entries 1440000
HT ID
QT board

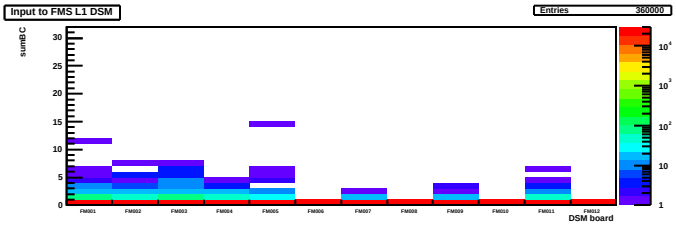

Input to FMS L0 DSM
Entries 59756
HT ID - simulated
QT board

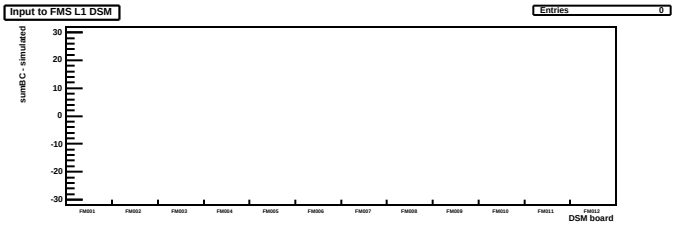

Input to FMS L1 DSM
Entries 360000
sumD
DSM board

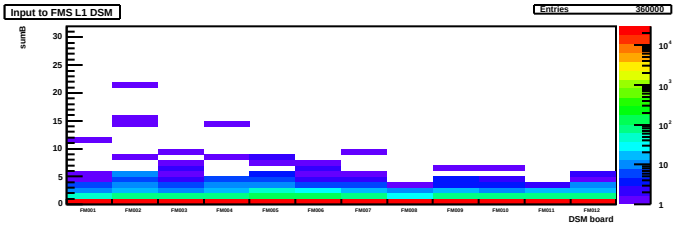

Input to FMS L1 DSM
Entries 0
sumD - simulated
DSM board

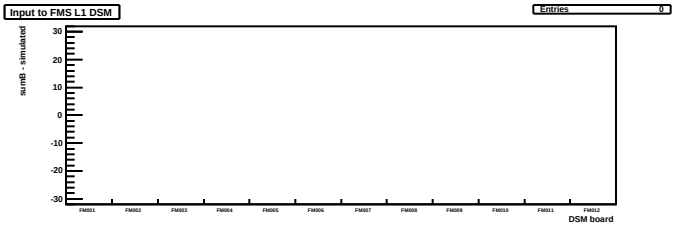

Input to FMS L1 DSM
Entries 360000
sumC
DSM board

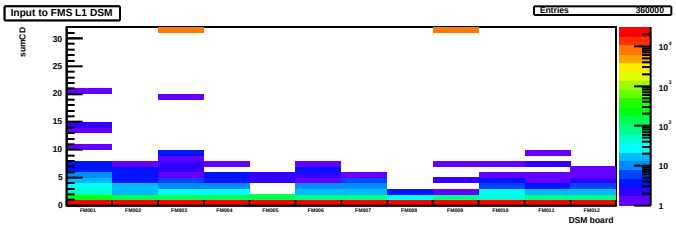

Input to FMS L1 DSM
Entries 2
sumC - simulated
DSM board

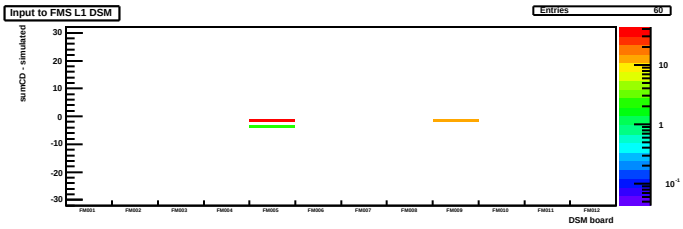

Input to FMS L1 DSM
Entries 360000
sumBC
DSM board

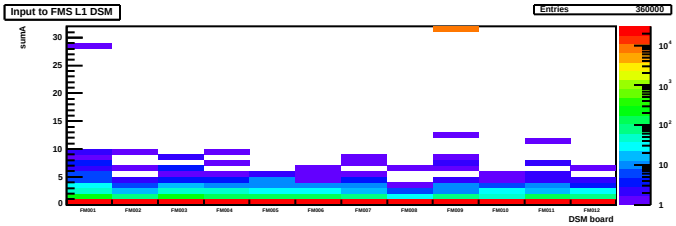

Input to FMS L1 DSM
Entries 0
sumBC - simulated
DSM board

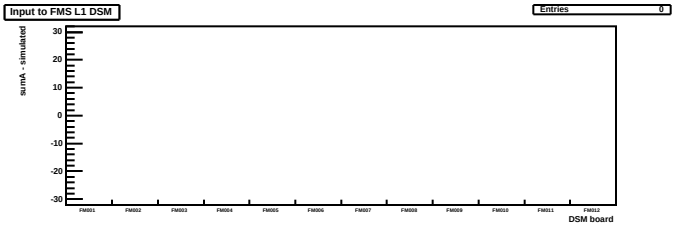

Input to FMS L1 DSM
Entries 360000
sumB
DSM board

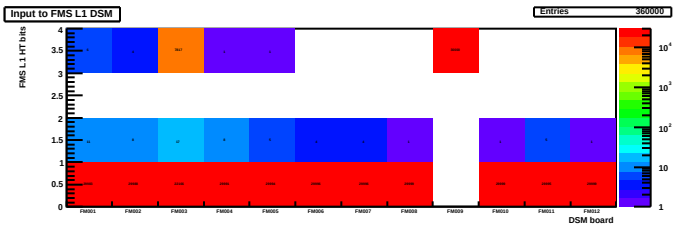

Input to FMS L1 DSM
Entries 0
sumB - simulated
DSM board

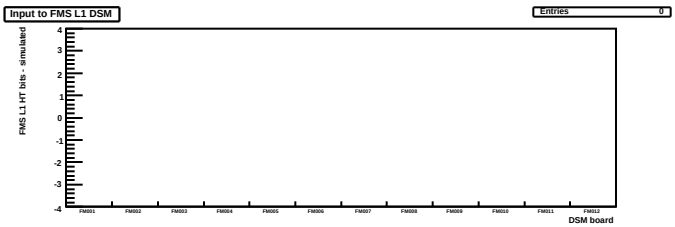

Input to FMS L1 DSM
Entries 360000
sumCD
DSM board

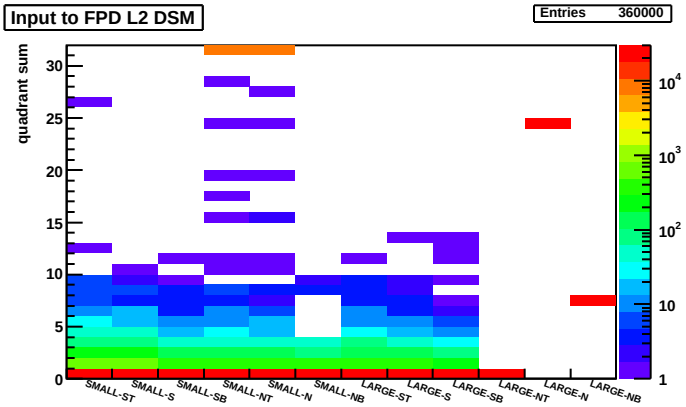

Input to FMS L1 DSM
Entries 60
sumCD - simulated
DSM board

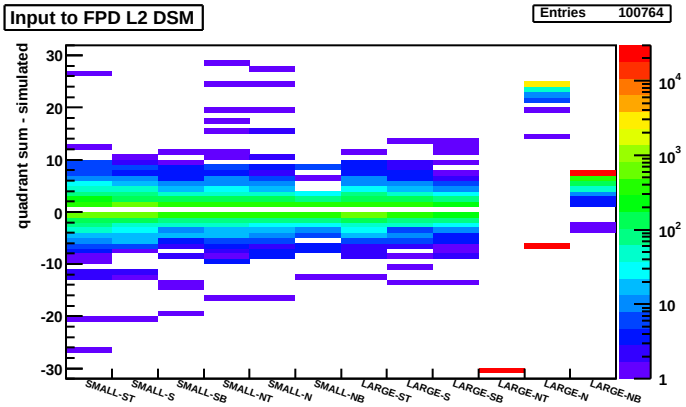

Input to FMS L1 DSM
Entries 360000
sumA
DSM board

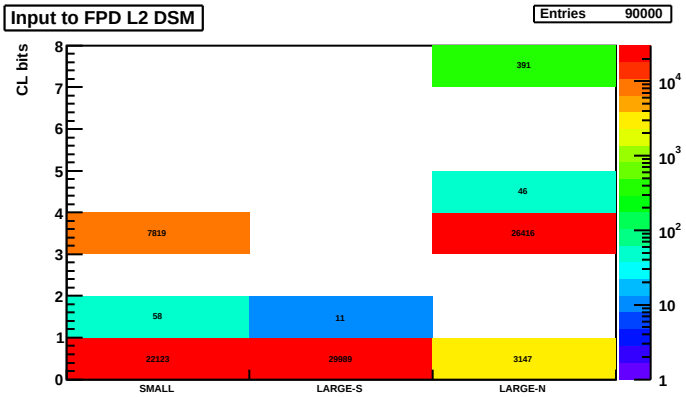

Input to FMS L1 DSM
Entries 0
sumA - simulated
DSM board

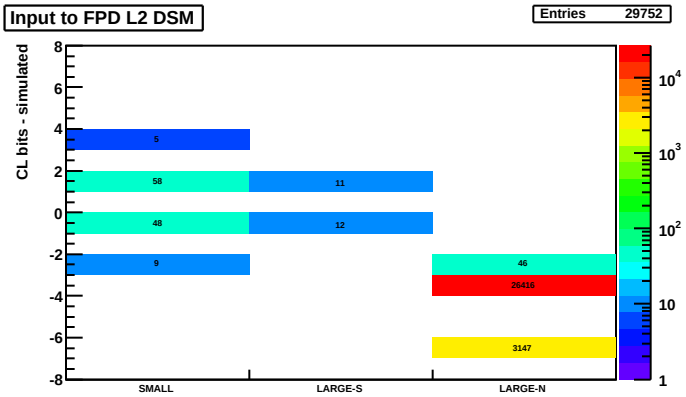

Input to FMS L1 DSM
Entries 360000
FMS L1 HT bits
DSM board

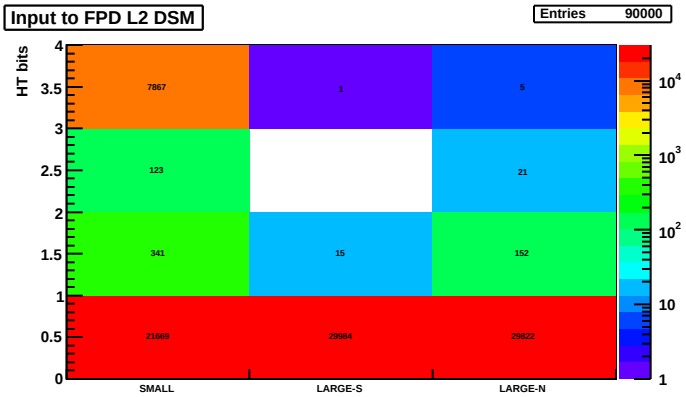

Input to FMS L1 DSM
Entries 0
FMS L1 HT bits - simulated
DSM board

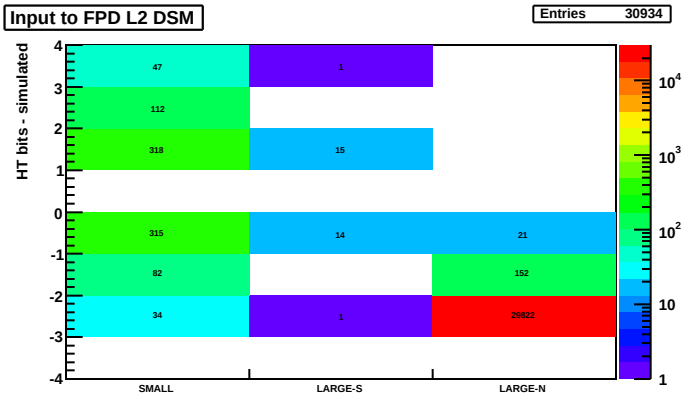

Input to FPD L2 DSM
Entries 360000
quadrant sum
SMALL-ST
SMALL-S
SMALL-SB
SMALL-NT
SMALL-N
SMALL-NB
LARGE-ST
LARGE-S
LARGE-SB
LARGE-NT
LARGE-N
LARGE-NB

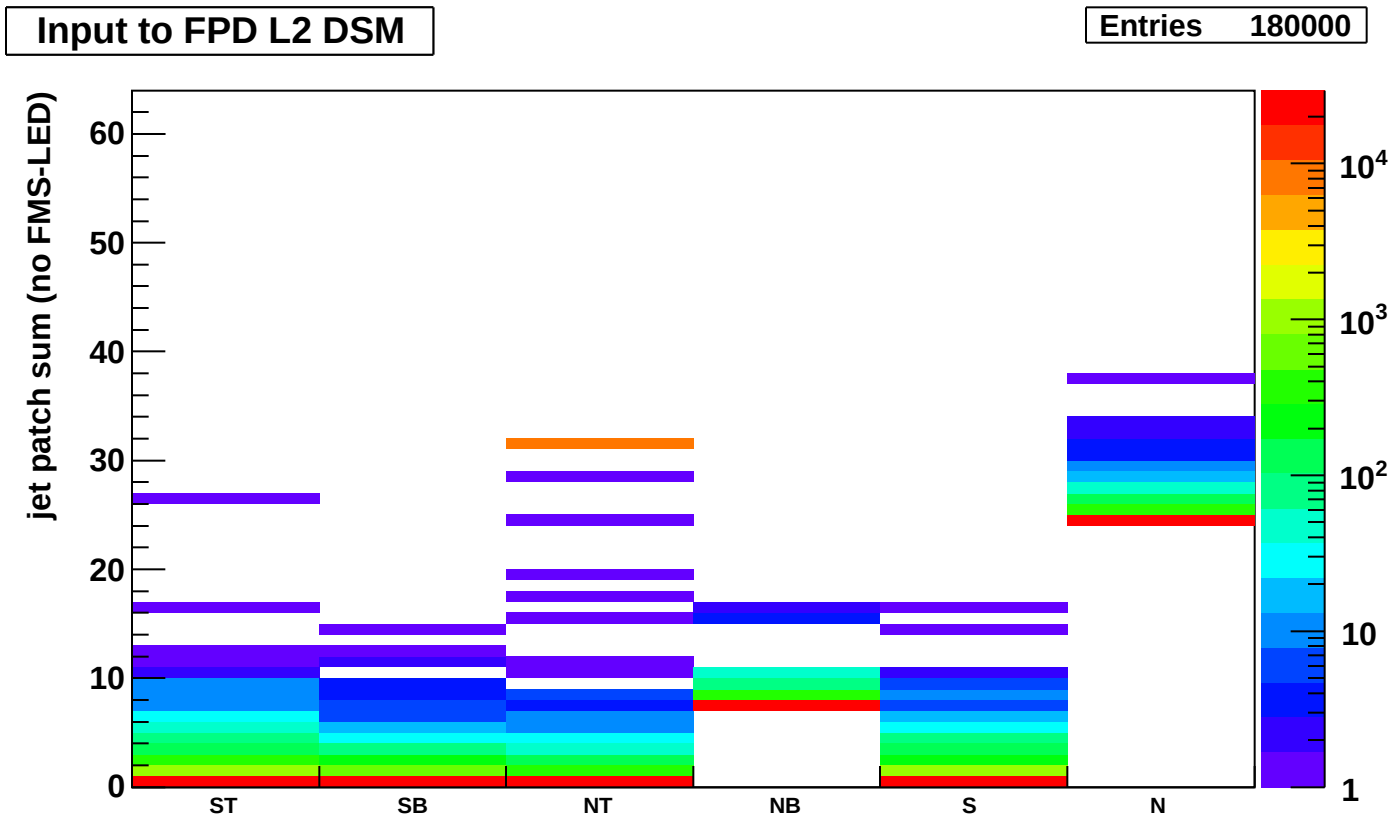

Input to FPD L2 DSM
Entries 100764
quadrant sum - simulated
SMALL-ST
SMALL-S
SMALL-SB
SMALL-NT
SMALL-N
SMALL-NB
LARGE-ST
LARGE-S
LARGE-SB
LARGE-NT
LARGE-N
LARGE-NB

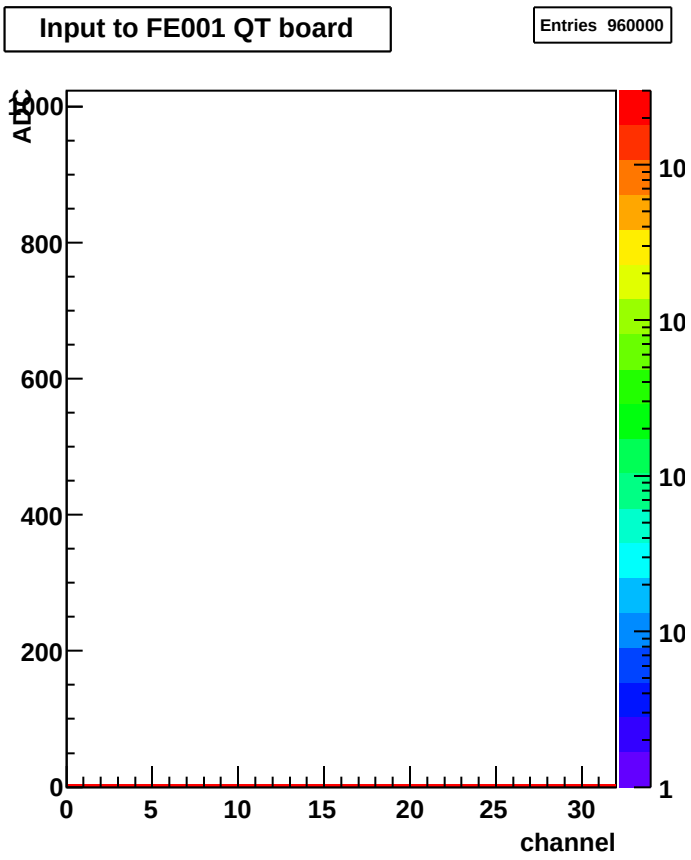

Input to FPD L2 DSM
Entries 90000
CL bits
391
46
7819
26416
58
11
22123
29989
3147
SMALL
LARGE-S
LARGE-N

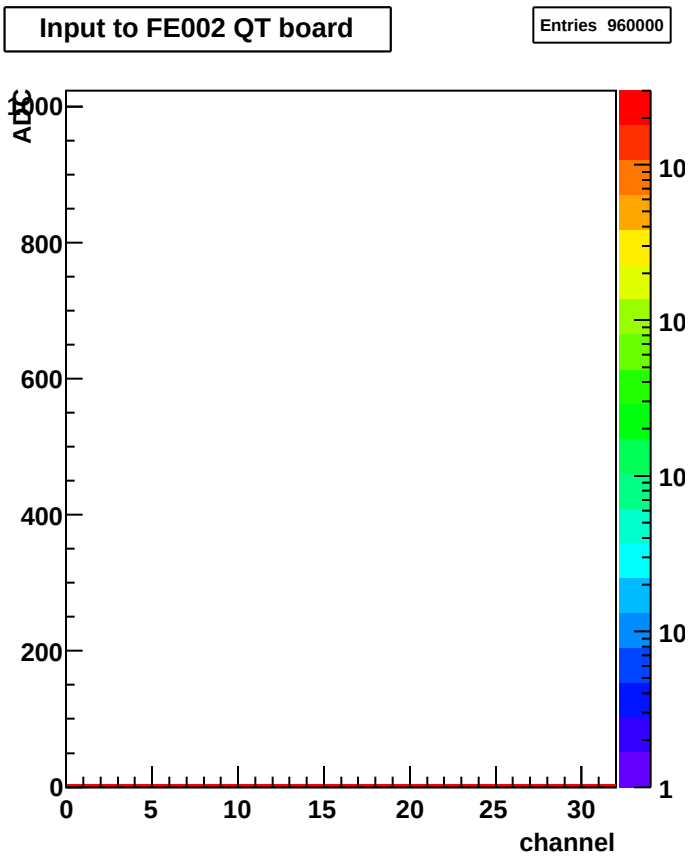

Input to FPD L2 DSM
Entries 29752
CL bits - simulated
5
58
11
48
12
9
46
26416
3147
SMALL
LARGE-S
LARGE-N

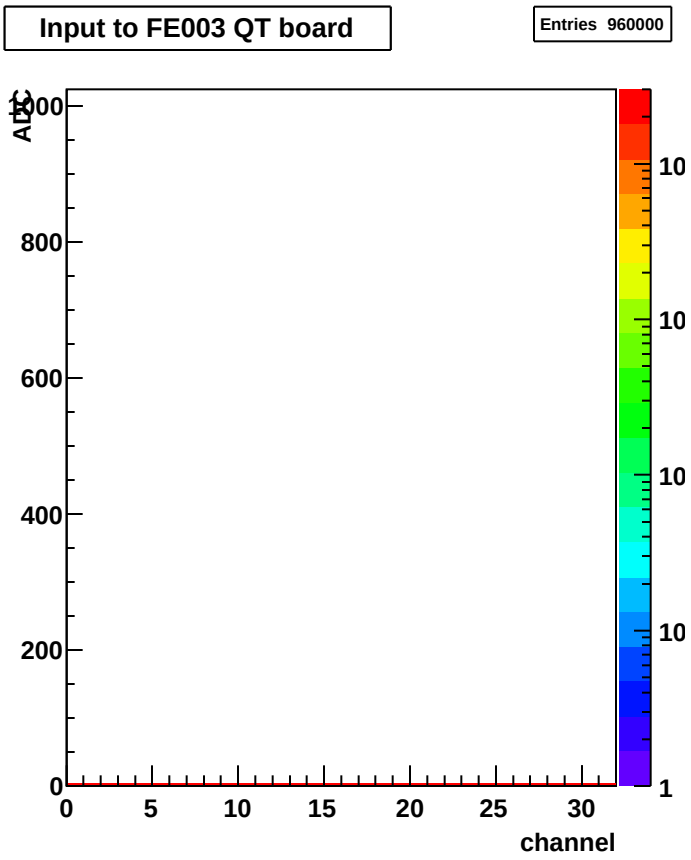

Input to FPD L2 DSM
Entries 90000
HT bits
7867
1
5
123
21
341
15
152
21669
29984
29822
SMALL
LARGE-S
LARGE-N

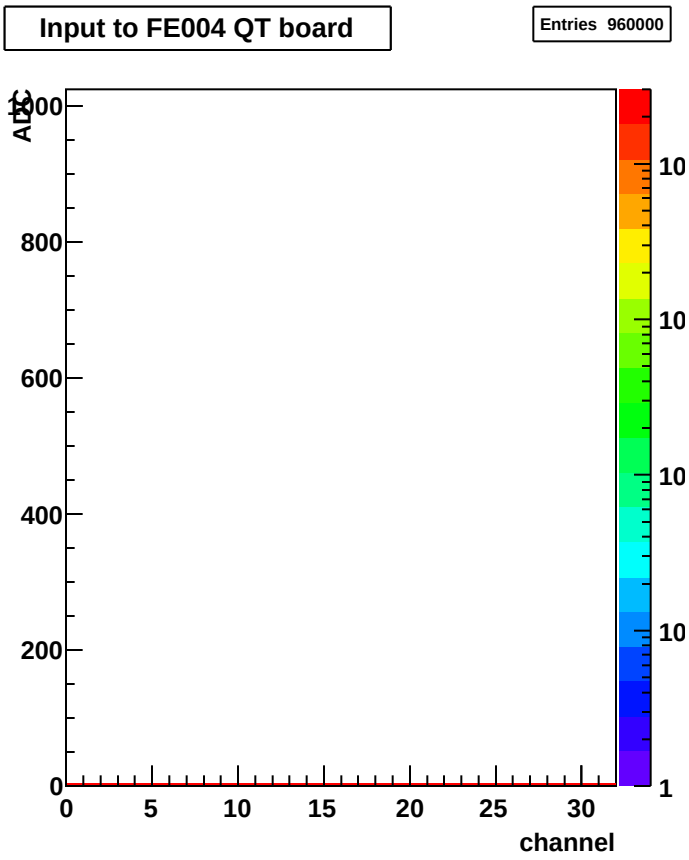

Input to FPD L2 DSM
Entries 30934
HT bits - simulated
47
1
112
318
15
315
14
21
82
152
34
1
29822
SMALL
LARGE-S
LARGE-N

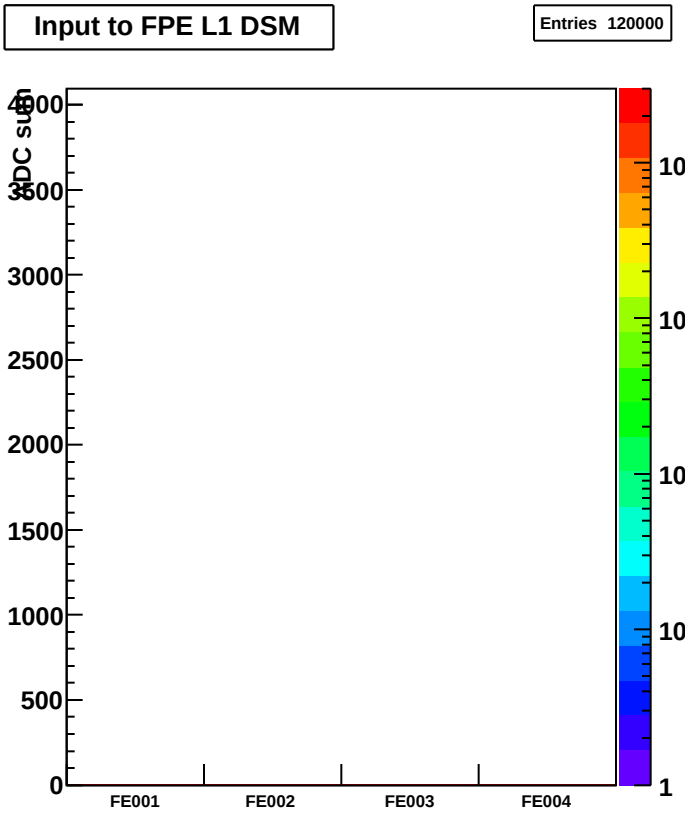

Input to FPD L2 DSM
Entries 180000
jet patch sum (no FMS-LED)
0
10
20
30
40
50
60
ST
SB
NT
NB
S
N
1
10
10^2
10^3
10^4

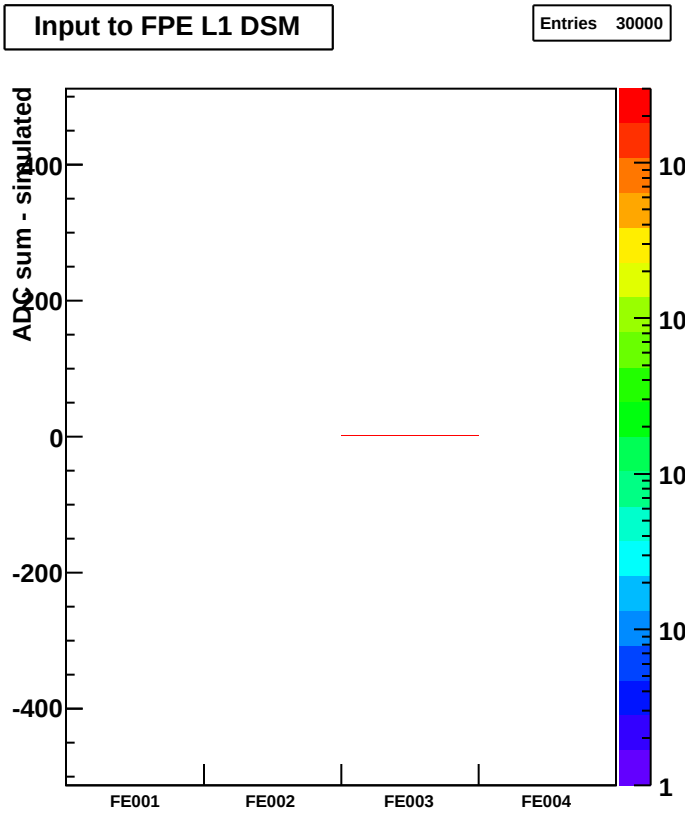

Input to FE001 QT board
Entries 960000
ADC
channel

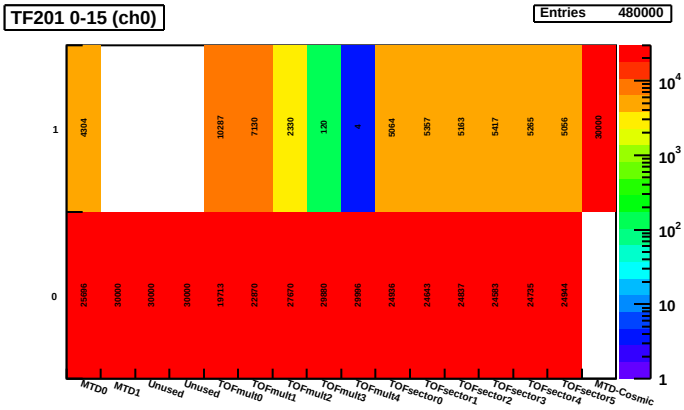

Input to FE002 QT board
Entries 960000
ADC
channel

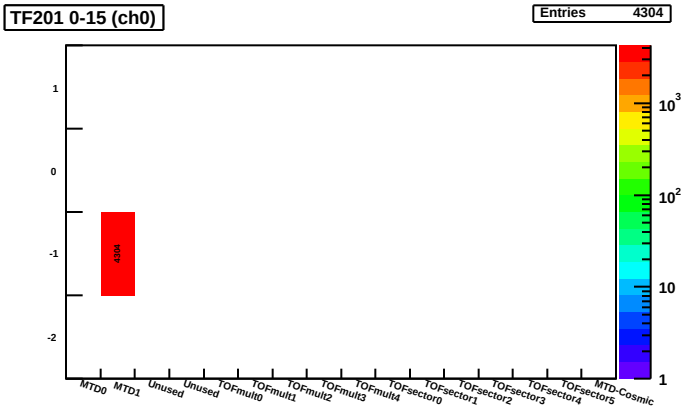

Input to FE003 QT board
Entries 960000
ADC
channel

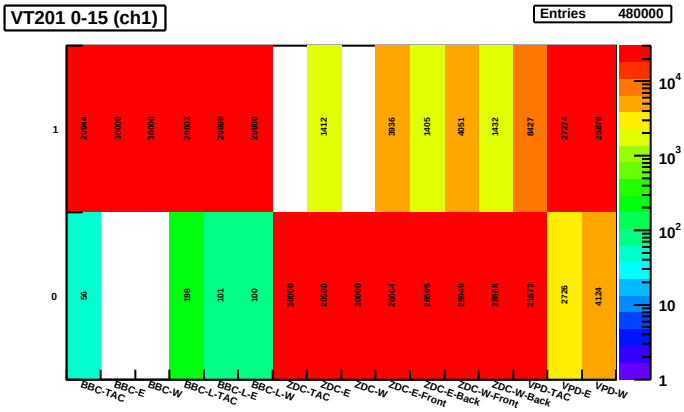

Input to FE004 QT board
Entries 960000
ADC
channel

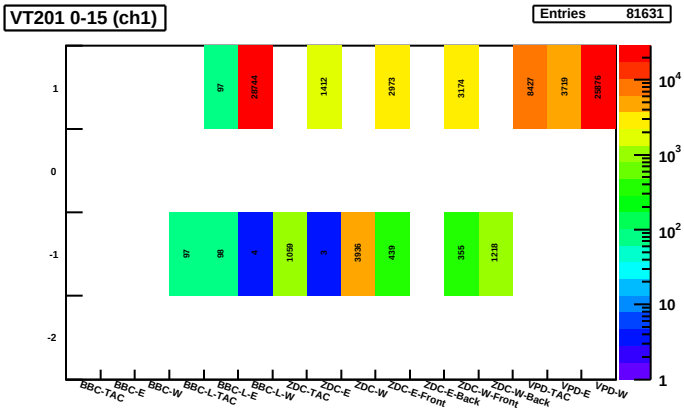

Input to FPE L1 DSM
Entries 120000
ADC sum
4000
3500
3000
2500
2000
1500
1000
500
0
FE001
FE002
FE003
FE004
10
10
10
10
1

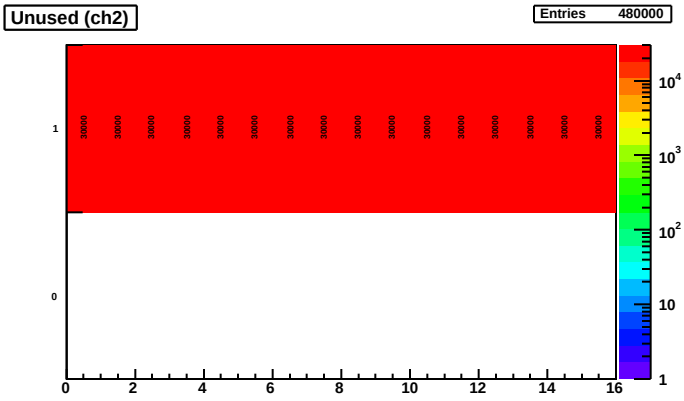

Input to FPE L1 DSM
Entries 30000
ADC sum - simulated
0
-200
-400
FE001
FE002
FE003
FE004
10
10
10
10
1

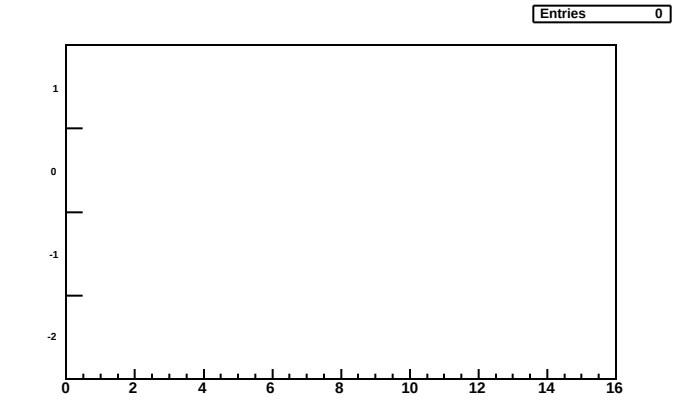

TF201 0-15 (ch0)
Entries 480000
MTD0 MTD1 Unused Unused TOFmult0 TOFmult1 TOFmult2 TOFmult3 TOFmult4 TOFsector0 TOFsector1 TOFsector2 TOFsector3 TOFsector4 TOFsector5 MTD-Cosmic

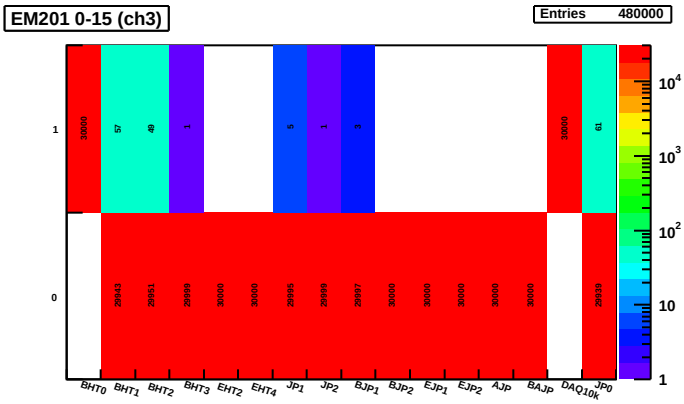

TF201 0-15 (ch0)
Entries 4304
MTD0 MTD1 Unused Unused TOFmult0 TOFmult1 TOFmult2 TOFmult3 TOFmult4 TOFsector0 TOFsector1 TOFsector2 TOFsector3 TOFsector4 TOFsector5 MTD-Cosmic


VT201 0-15 (ch1)
Entries 480000
BBC-TAC BBC-E BBC-W BBC-L-TAC BBC-L-E BBC-L-W ZDC-TAC ZDC-E ZDC-W ZDC-E-Front ZDC-E-Back ZDC-W-Front ZDC-W-Back VPD-TAC VPD-E VPD-W


VT201 0-15 (ch1)
Entries 81631
BBC-TAC BBC-E BBC-W BBC-L-TAC BBC-L-E BBC-L-W ZDC-TAC ZDC-E ZDC-W ZDC-E-Front ZDC-E-Back ZDC-W-Front ZDC-W-Back VPD-TAC VPD-E VPD-W


Unused (ch2)
Entries 480000


Entries 0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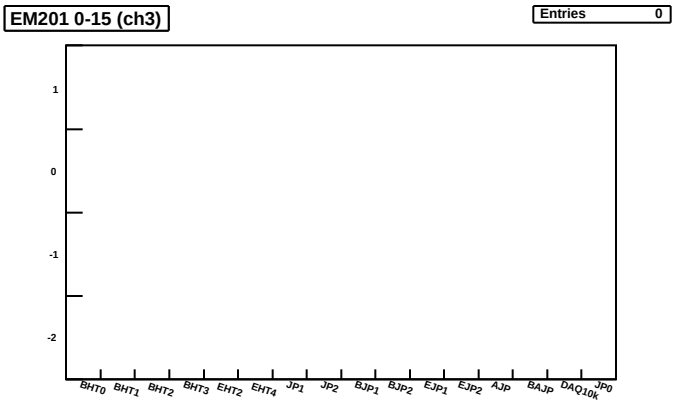
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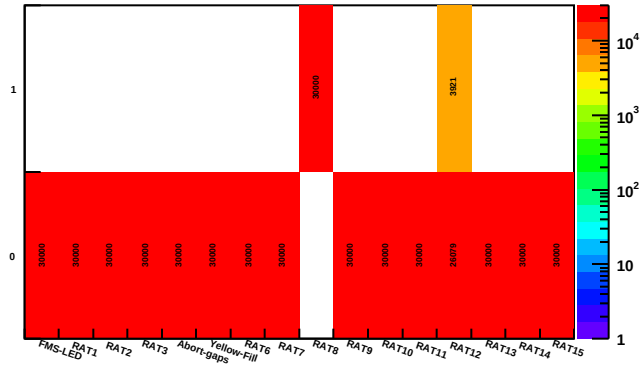
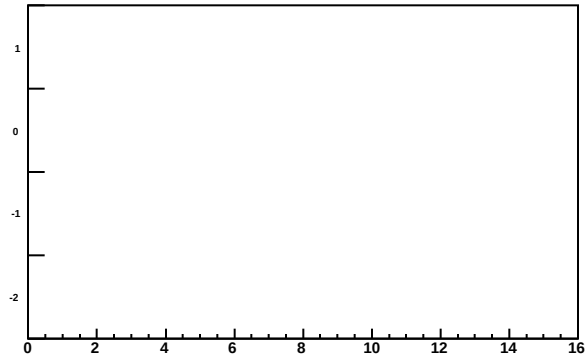
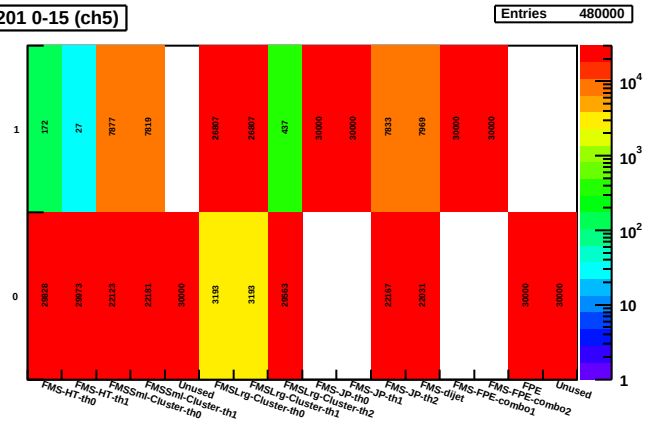
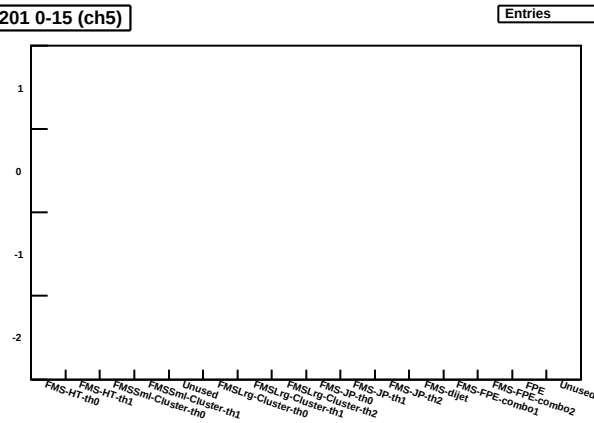
RAT board (ch4)



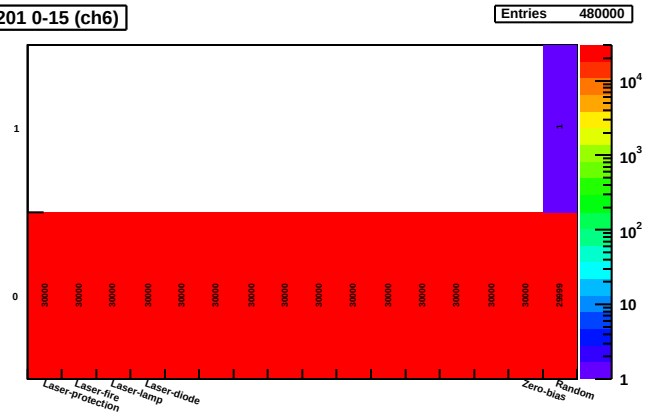


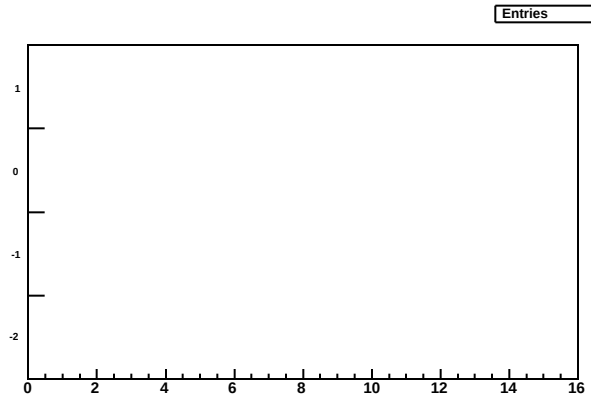
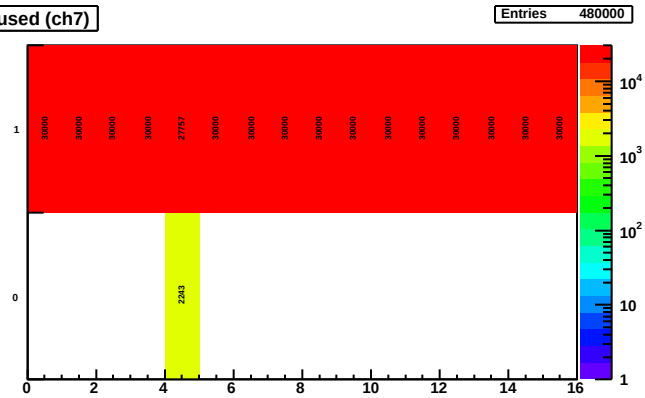
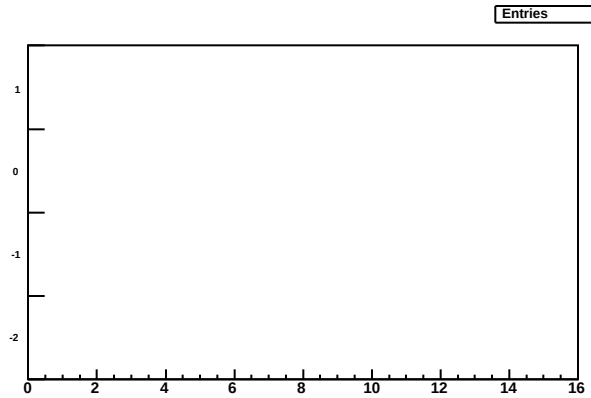
FP201 0-15 (ch5)





ST201 0-15 (ch6)





Unused (ch7)